# *Models 585/588 Microwave Pulse Counters*

## *Service*

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# Section 5
# Adjustment and Calibration

## INTRODUCTION

To adjust the 585 or 588 counter correctly, use the procedures described in the following paragraphs. The recommended calibration interval is 6 months. Additional adjustments should be made if the counter does not operate as specified, or if it has been repaired. If the adjustments do not result in the specified performance, refer to the troubleshooting section of this manual.

The adjustment and calibration procedure comprises five calibrations:

1. Power supply adjustment
2. Time-base adjustment
3. Band 2 YIG DAC Automatic Calibration
4. Gate error calibration
5. Display intensity adjustment

Calibrations 1, 2, and 5 require removal of the top cover for adjustment. The display intensity adjustment is for user comfort only and need not be performed.

Table 5-1 describes the functions, specifications, and methods to be used when the adjustment and calibration routines are performed.

## Table 5-1. Procedure Description

| FUNCTION | PERFORMANCE SPECIFICATION | METHOD |
|---|---|---|
| Power Supply Adjustment | Voltage between A2TP1 (+12 V) and ground is +12 ±0.01 V. | Adjust at A2R3 Check with DVM |
| | Voltage between A2TP2 (-12 V) and ground is -12 ±0.01 V. | Adjust at A2R6 check with DVM |
| Time Base | Adjust the output frequency of the TCXO to 10 MHz ±0.1 Hz | Turn the TCXO calibration screw, check count output with 545B counter |
| YIG DAC Calibration | Auto-calibration of DAC to YIG filter | Use Special Function 91 |
| Gate Error Calibration | Gate error is ±0.05 times the gate width | Use Special Function 92 to calibrate gate error in each band |
| Display Intensity | CRT brightness level is adjusted to suit operator's comfort | Adjust A12A2R4 on Front Panel Logic Board |

## TEST EQUIPMENT

Minimum use specifications are the principal parameters required for performance of the calibration, and are included to assist in the selection of alternate equipment. Satisfactory performance of alternate items should be verified prior to use. All applicable equipment must bear evidence of current calibration.

### Table 5-2. Equipment Description

| DESCRIPTION | CRITICAL PARAMETER | MFR | MODEL |
|---|---|---|---|
| Microwave Counter | 0.1 Hz resolution | EIP | 545B |
| Digital Voltage Meter | 4 1/2 digit resolution | Fluke | 8050A |
| Pulse Generator | 20-ns pulses | Wavetek | 801 |
| 50-ohm Feedthrough Termination | 50 ohms resistance | Pamona | 4119-50 |
| Oscilloscope | 100 MHz Bandwidth | Tektronix | 475 |
| Frequency Extender | 26.5 - 60 GHz range | Watkins Johnson | 1204-42 |
| Microwave Synthesizer | 10 MHz to 26.5 GHz | HP | 8340A |

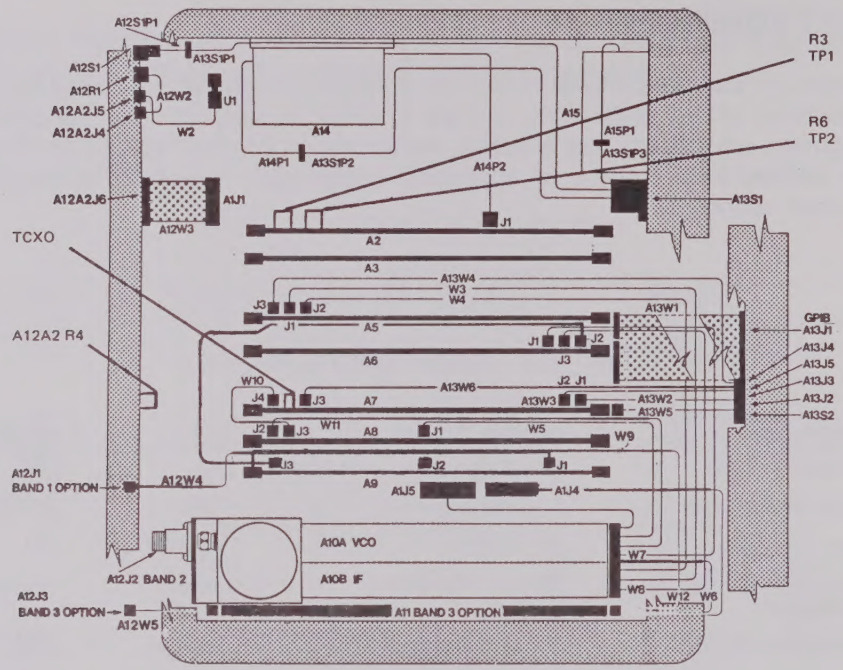



Figure 5-1. Adjustment Locations

## PRELIMINARY OPERATIONS

Review the entire procedure before starting the calibration. Connect the instrument to local line voltage and turn on. Allow 5 minutes for the instrument to warm up before starting any procedure. Set the instrument controls to their default values by pressing the "INIT" key.

# CALIBRATION PROCESS

## POWER SUPPLY ADJUSTMENT

### EQUIPMENT

Digital Voltmeter Fluke 8050A

Figure 5-2. Power Supply Adjustment

### PROCEDURE

1. Set up equipment as shown in Figure 5-2.
2. Remove the top cover. Turn the counter on and let it warm up for five minutes. The following voltage adjustments are done on the Power Supply board (A2).
3. Connect the digital volt meter (DVM) between A2TP1 (+12) and ground.
4. Adjust A2R3 until the voltage measures +12.000 ±0.01 Vdc.
5. Connect the DVM between A2TP2 (-12 Volts) and ground.
6. 6. Adjust A2R6 until the voltage measures -12.000 ±0.01 Vdc.

## TIME BASE CALIBRATION

The time base oscillator used in the counter is a 10-MHz temperature-compensated crystal oscillator (TCXO). The accuracy of this oscillator directly affects the measurement accuracy of the counter. From the time an oscillator is set to its specified frequency it will begin drifting. The magnitude of this drift is specified as the aging rate of the oscillator. Time base calibration adjusts for this drift and should be performed at least every 6 months.

The procedure described on the next page uses an EIP Model 545B Microwave Frequency Counter to measure the frequency of the time base. The 545B was chosen because it provides a 0.1 Hz resolution in Band 1. The external reference input on the 545B must be connected to a 10 MHz frequency standard. The accuracy of the standard should be several orders of magnitude better than the TCXO.

## EQUIPMENT

| | |
|---|---|
| Microwave Counter | EIP 545B |
| 50-ohm Feedthrough Termination | Pamona |

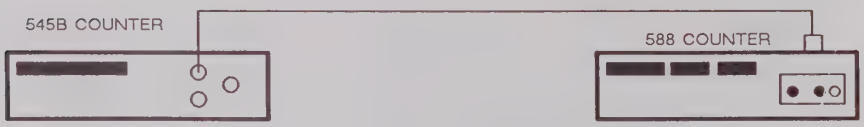



Figure 5-3. Time Base Calibration

## PROCEDURE

1. Set up equipment as shown in Figure 5-3.

2. Remove the top cover. Turn the counter on and let the counter warm up for 15 minutes.

3. Connect the signal from the 10 MHz IN/OUT connector on the rear panel of the 585/588 through a 50-ohm feedthrough termination to the Band 1 input of an EIP 545B counter. Select 0.1 Hz resolution on the 545B by pressing the "RES" key followed by the decimal point key and then the 1 key. make sure that IN/EXT switch on the rear panel of the 585/588 in the internal position.

4. Connect a 10 MHz frequency standard to the 10 MHz TIME BASE (external reference) input connector on the rear panel of the EIP 545B counter. On the 545B, set the 10 MHz INT/EXT switch to the EXT position.

5. Adjust the TCXO (on the gate generator board) to 10 MHz +/- 0.1 Hz. The frequency of the TCXO is adjusted by turning the adjustment screw located on the top of the TCXO case.

## YIG DAC AUTOMATIC CALIBRATION

This counter uses an electronically tunable microwave band-pass filter (YIG) on the Band 2 input. This filter is called a YIG because of the type of material used in its construction. The frequency that the filter is tuned to is controlled by a digital to analog converter (DAC). The YIG DAC calibration develops a table of correction factors that correlate the digital information sent to the DAC to the frequency that the YIG filter is tuned to.

When this function is activated, the counter will display F1 and measure a user-supplied 2 GHz input. Then it will display F2, wait for the user to change the input to 18 GHz, and measure it. The counter then calculates and stores (in non-volatile memory) the correction factors for the YIG DAC.

**CAUTION**

**Care must be used when operating Special Function 91. Although the counter cannot be damaged by this function, improper operation of it can affect the counter calibration, possibly rendering the counter unusable until it can be recalibrated. Do not call this function unless familiar with its operation.**

To calibrate the YIG DAC:

1. Apply a signal at 2 GHz ±2 MHz at approximately 0 dBm to the Band 2 input connector.
2. Call Special Function 91, when the counter displays F1 press the TRIG key.
3. When the display changes from F1 to F2, apply a signal at 18 GHz ±2 MHz, at approximately 0 dBm and press the TRIG key.
4. When the display returns to normal, the counter YIG DAC is calibrated.

## GATE ERROR CALIBRATION

The purpose of this adjustment is to reduce the gate error. Each time the gate is terminated, it is statistically possible to be off by one count, which is added to the frequency count. In pulsed frequency measurement the shorter the pulse width, the more gates are accumulated (in order to obtain the needed resolution); therefore the total error is proportional to the number of times the gate is cycled (inversely proportional to the gate width). The error is systematic and is not reduced by frequency averaging. This error is affected by both input frequency and ambient temperature.

Performing this adjustment at room temperature (25°C) will guarantee performance to specifications over the temperature range of the counter. If the counter is to be used at a temperature other than 25°C, performance may be improved by performing this calibration at that temperature.

Gate widths less than 20 ns (less than 50-ns pulse widths) are subjected to constant erroneous readings. If such a gate width is desired, performance may be improved by performing a special calibration for this gate width at the required frequency. This calibration may be performed without removing the covers from the instrument.

### EQUIPMENT

| | |
|---|---|
| Microwave Synthesizer | Hewlett Packard 8340A |
| Pulse Generator | Wavetek 801 |
| 50-ohm Feedthrough Termination | Pamona |
| Oscilloscope | Tektronix 475 |

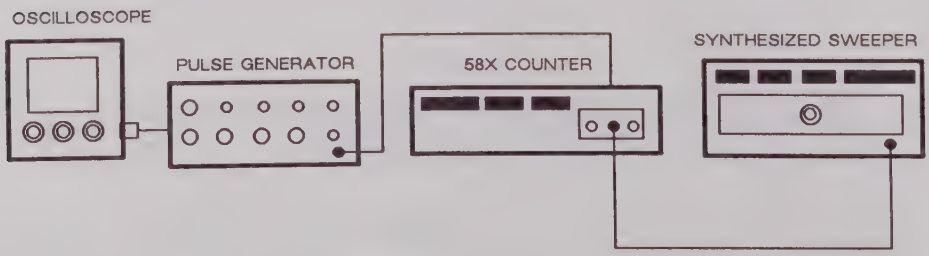



Figure 5-4. Band 1 and 2 Gate Error Calibration

## BAND 2 GATE ERROR CALIBRATION

### PROCEDURE

1. Set up equipment as shown in Figure 5-4.
2. Apply a CW signal between 2 and 10 GHz at approximately 0 dBm to the BAND 2 input connector.
3. Connect the pulse generator to the oscilloscope through a 50-ohm feed-through at the oscilloscope). Set the pulse generator as follows: 1 MHz PRF, 50 ns complementary pulse width, base line at zero volts, and amplitude at -1 volt. Connect the pulse generator (without the feed-through) to the INHIBIT INPUT connector on the rear panel of the counter.
4. Press keys for SPECIAL FUNCTION 92, then press Trigger key. The counter is in the autocalibrate state for about 1 minute.

## BAND 1 GATE ERROR CALIBRATION (Option 5802)

### PROCEDURE

1. Set up equipment as shown in Figure 5-4, and adjust as specified in step 3, Band 2 Calibration
2. Press BAND 1 key. Apply a CW signal at 650 MHz, 0 dBm to the BAND 1 input connector.
3. Press keys for SPECIAL FUNCTION 92, then press Trigger key. The counter is in the autocalibrate state for about 1 minute.

## BAND 3 GATE ERROR CALIBRATION (Option 5804)

### EQUIPMENT

| | |
|---|---|
| Microwave Synthesizer | Hewlett Packard 8340A |
| Pulse Generator | Wavetek 801 |
| 50-ohm Feedthrough | Pamona |
| Oscilloscope | Tektronix 475 |
| Frequency Extender | Watkins Johnson 1204-42 |

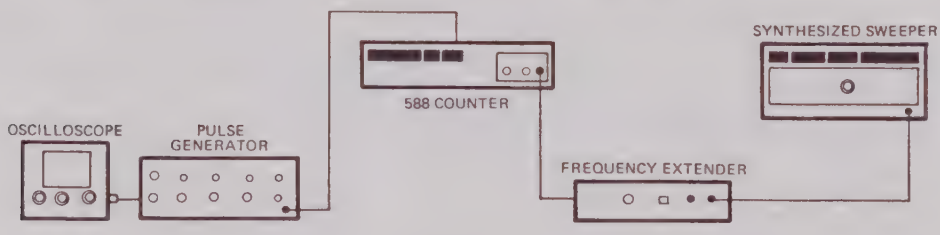



Figure 5-5. Band 3 Gate Error Calibration

### PROCEDURE

1. Set up equipment as shown in Figure 5-5.
2. Using the appropriate remote sensor, apply a CW signal to the BAND 3 input connector of the counter.
3. Select Band 3 and the appropriate sub-band.
4. Adjust equipment as in step 3, Band 2 Calibration.
5. Press the keys for SPECIAL FUNCTION 92. The counter is in the autocalibrate state for about 1 minute.

NOTE:

**Band 3 need not be calibrated for every sub-band. Calibration of any sub-band is sufficient for all of Band 3.**

## DISPLAY INTENSITY ADJUSTMENT

An adjustment (A12A2R4) is provided on the Front Panel Logic board for display intensity; it may be adjusted for most comfortable viewing.

# Section 6
# Troubleshooting

## INTRODUCTION

This section defines troubleshooting aids that can be used with the 585/588 counter. They are:

- Signature analysis
- Self diagnostics
- Keyboard controlled circuit tests

The procedures and tables are provided for troubleshooting to a functional circuit level.

## SIGNATURE ANALYSIS

Signature analysis is a technique used to troubleshoot complex logic circuitry. It uses data compression to reduce any data pattern to a four-character alphanumeric word.

The start and stop inputs define the measurement window. Each time a transition within the measurement window occurs on the clock input, the probe is sampled, and the logic level is shifted into the analyzer. This information is used to generate a signature unique to that data string. That signature can then be compared to a reference signature, taken from a known good product, to determine if the data string is correct. The counter implements signature analysis in either a free running or program controlled manner.

## FREE RUNNING

When performing signature analysis the microprocessor board is set up in a free running mode by moving the header in A3 E1 to A3 E2. Free running means forcing a simple instruction such as NOP on the data bus, which the microprocessor sees at every address location. This causes the microprocessor to continually cycle through its entire address range, accessing everything on the address bus as it does. By strategically placing the start and stop connections from the signature analyzer, the user can probe the entire bus system for bad signatures.

Table 6-1. Microprocessor Free Running Signatures

| | Start | Stop | Clock |
|---|---|---|---|
| Connections | A3 TP4 | A3 TP4 | A3 TP3 |
| Buttons | In | In | In |

| Line | Signature | Line | | Signature |
|---|---|---|---|---|
| A0 (P1 Pin 54) | UUUU | U5 | Pin 6 | 76AC |
| A1 (P1 Pin 53) | FFFF | U5 | Pin 8 | 0000 |
| A2 (P1 Pin 52) | 8484 | U5 | Pin 12 | 65F5 |
| A3 (P1 Pin 51) | P763 | | | |
| A4 (P1 Pin 50) | 1U5P | | | |
| A5 (P1 Pin 49) | 0356 | | | |
| A6 (P1 Pin 48) | U759 | | | |
| A7 (P1 Pin 47) | 6F9A | | | |
| A8 (P1 Pin 46) | 7791 | | | |
| A9 (P1 Pin 45) | 6321 | | | |
| A10 (P1 Pin 44) | 37C5 | | | |
| A11 (P1 Pin 43) | 6U28 | | | |
| A12 (P1 Pin 42) | 4FCA | | | |
| A13 (P1 Pin 41) | 4868 | | | |
| A14 (P1 Pin 40) | 9UP1 | | | |
| A15 (P1 Pin 39) | 00001 | | | |
| U3 Pin 7 | 76AC | | | |
| TP6 | 854F | | | |
| TP7 | PACH | | | |
| TP8 | 755F | | | |
| TP9 | 755H | | | |
| U8 Pin 19 | U3P7 | | | |
| U9 Pin 18 | 0003 | | | |
| U10 Pin 18 | 0003 | | | |
| U17 Pin 1 | 9F14 | | | |
| U17 Pin 2 | 9F17 | | | |

NOTE
The Signatures shown were taken using the HP 5004A Signature Analyzer

+5V 0003, phase 2 0003 *

* Due to the synchronous qualities of the signature analyzer, phase 2 will read the same as + 5V but the logic probe will be flashing. Likewise, anything gated with phase 2 may have the same signature as the ungated signal.

## SELF DIAGNOSTICS

At turn-on, the counter performs several internal diagnostic checks, checking the RAM, PROM, and the associated decoding circuitry. The display shows dashes during these checks. If the counter passes the tests, it then enters the normal operating mode. If the counter fails any checks, an error message will be displayed. Please refer to Table 6-2.

Table 6-2. Self Diagnostic Error Indications

| Problem | Error Message |
|---|---|
| RAM Bad | 60 |
| A3 U11 (Basic Program) Bad | 61 |
| A3 U12 (Basic Program) Bad | 62 |
| A3 U13 (Basic Program) Bad | 63 |

## KEYBOARD CONTROLLED CIRCUIT TESTS

There are seven keyboard-controlled circuit tests (01 through 07). All tests are accessed by pressing SPECIAL FUNC and the two digit test number. Tests that do not require keyboard inputs to function (tests 01, 02, 03, 04, 06, 07) can be exited by pressing any key. This causes the counter to exit the test and enter the functions selected. Test 05, which uses the keyboard in its operation, can be exited by pressing CLEAR DISPLAY. This causes the counter to return to normal operation.

01 **100 MHz Self Test.** This test sets the VCO to 400 MHz, divides it by four, and counts the 100 MHz output from the divider. It checks the count chain, VCO and VCO phase lock circuitry, and the gate generator.

02 **Display 8s Test.** This test lights all LEDs, annunciators, and decimal points. It checks that everything on the display is operational.

03 **Display Segment Test.** This test lights each segment of each digit and each annunciator one at a time, cycling through all segments. The cycle rate can be adjusted with the sample rate pot. It verifies that each segment of the display, segment drivers, and display multiplexer operate properly and independently.

04 **Display Digit Test.** This test lights one entire digit, and its decimal point, at a time. It cycles through all digits and annunciators. The cycle rate is determined by the sample rate pot. It checks each digit and digit driver independently, and verifies operation of the display multiplexer.

05 **Keyboard Test.** This test displays the key code of each key as it is pressed. Test 05 checks the keyboard, keyboard interrupt, and keyboard decode circuitry. The key codes (coordinates) for each key are shown in Table 6-3.

Table 6-3. Keyboard Test Coordinates

| Key | Key Code |
|---|---|
| 7 | 11 |
| 8 | 12 |
| 9 | 13 |
| GHz | 14 |
| 4 | 21 |
| 5 | 22 |
| 6 | 23 |
| MHz | 24 |
| 1 | 31 |
| 2 | 32 |
| 3 | 33 |
| kHz | 34 |
| ± | 41 |
| 0 | 42 |
| . | 43 |
| Hz | 44 |
| PULSE WIDTH | 51 |
| PULSE PERIOD | 52 |
| CLEAR DATA | 53 |
| INIT/LOCAL | 61 |
| CLR DISPLAY | EXIT TEST |

06 **PROM Check Sum Test.** This test generates the check sum for each PROM in the counter and compares it with the check sum stored in the firmware. If all the check sums generated are correct, the counter displays the word PASSED on the front panel. If any one of the check sums is incorrect, an error message corresponding to that particular check sum is output to the display.

07 **Display Counter Model Number.** This function shows the user whether the counter is configured as 585 or a 588.

## TROUBLESHOOTING TREES

Troubleshooting trees are intended only as a guide, and do not describe every possible failure situation. Turn power off before removing or installing any PC boards or connectors. If the following assemblies are repaired or replaced, recalibration of the counter will be necessary.

- A2 Power Supply
- A3 Microprocessor
- A6 Count Chain
- A7 Gate Generator
- A8 Converter Control
- A10 Band 2 Converter Assembly

**CAUTION**

**Do not attempt to repair or disassemble the A10 hybrid assembly.**

## TEST EQUIPMENT REQUIRED

Table 6-4. Troubleshooting Test Equipment

| Manufacturer | Model | Description | Critical Parameters |
|---|---|---|---|
| Tektronix | 475 | Oscilloscope | 100 MHz min. Bandwidth |
| Fluke | 8050A | Digital Voltmeter | 4-1/2 digit resolution |
| Hewlett Packard | 8559A/ 853A | Spectrum Analyzer | 6 GHz |
| Hewlett Packard | 5004A | Signature Analyzer | |
| Wavetek | 801 | Delay Pulse Generator | |
| HP | 8340A | Microwave Synthesizer | 10 MHz to 26.5 GHz |

To use the troubleshooting trees:

1. Refer to the main troubleshooting tree.
2. Step through the main troubleshooting tree, performing all necessary checks, until the failure mode is noted.
3. Refer to the appropriate troubleshooting tree for that failure mode.

Before servicing unit, verify that:

1. The line voltage and fuse are correct for the voltage setting.
2. The rear panel 10 MHz INT/EXT switch is set to internal.
   If the switch is set to external, check that a proper 10 MHz signal is applied to the 10 MHz IN/OUT connector.
3. The MIN PRF function is properly set. (See Section 3).
4. The counter is not inhibited by the rear panel inhibit input.

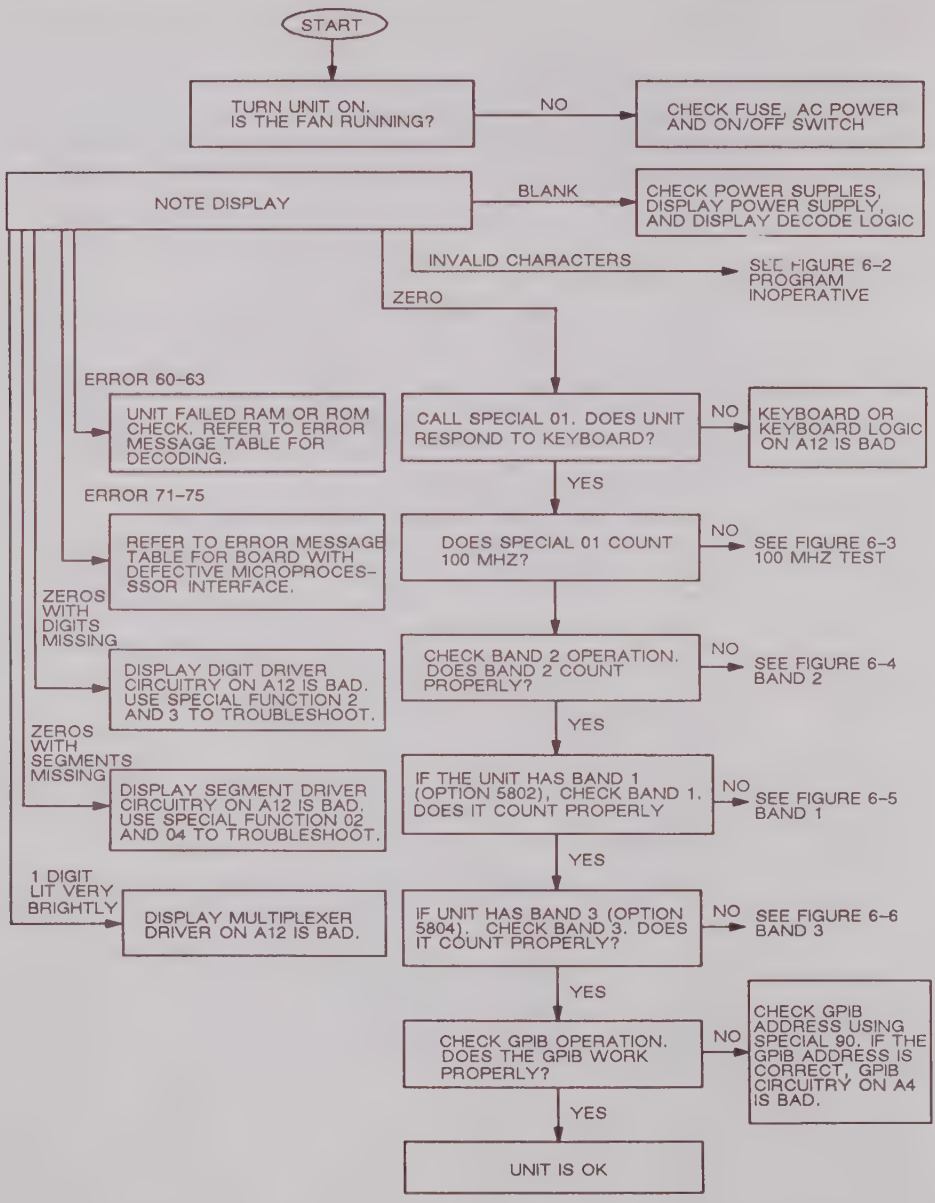

START
TURN UNIT ON. IS THE FAN RUNNING?
NO
CHECK FUSE, AC POWER AND ON/OFF SWITCH
NOTE DISPLAY
BLANK
CHECK POWER SUPPLIES, DISPLAY POWER SUPPLY, AND DISPLAY DECODE LOGIC
INVALID CHARACTERS
SEE FIGURE 6-2 PROGRAM INOPERATIVE
ZERO
ERROR 60-63
UNIT FAILED RAM OR ROM CHECK. REFER TO ERROR MESSAGE TABLE FOR DECODING.
CALL SPECIAL 01. DOES UNIT RESPOND TO KEYBOARD?
NO
KEYBOARD OR KEYBOARD LOGIC ON A12 IS BAD
YES
ERROR 71-75
REFER TO ERROR MESSAGE TABLE FOR BOARD WITH DEFECTIVE MICROPROCESSOR INTERFACE.
DOES SPECIAL 01 COUNT 100 MHZ?
NO
SEE FIGURE 6-3 100 MHZ TEST
ZEROS WITH DIGITS MISSING
DISPLAY DIGIT DRIVER CIRCUITRY ON A12 IS BAD. USE SPECIAL FUNCTION 2 AND 3 TO TROUBLESHOOT.
CHECK BAND 2 OPERATION. DOES BAND 2 COUNT PROPERLY?
NO
SEE FIGURE 6-4 BAND 2
YES
ZEROS WITH SEGMENTS MISSING
DISPLAY SEGMENT DRIVER CIRCUITRY ON A12 IS BAD. USE SPECIAL FUNCTION 02 AND 04 TO TROUBLESHOOT.
IF THE UNIT HAS BAND 1 (OPTION 5802), CHECK BAND 1. DOES IT COUNT PROPERLY
NO
SEE FIGURE 6-5 BAND 1
YES
1 DIGIT LIT VERY BRIGHTLY
DISPLAY MULTIPLEXER DRIVER ON A12 IS BAD.
IF UNIT HAS BAND 3 (OPTION 5804), CHECK BAND 3. DOES IT COUNT PROPERLY?
NO
SEE FIGURE 6-6 BAND 3
YES
CHECK GPIB OPERATION. DOES THE GPIB WORK PROPERLY?
NO
CHECK GPIB ADDRESS USING SPECIAL 90. IF THE GPIB ADDRESS IS CORRECT, GPIB CIRCUITRY ON A4 IS BAD.
YES
UNIT IS OK

Figure 6-1. Main Troubleshooting Tree

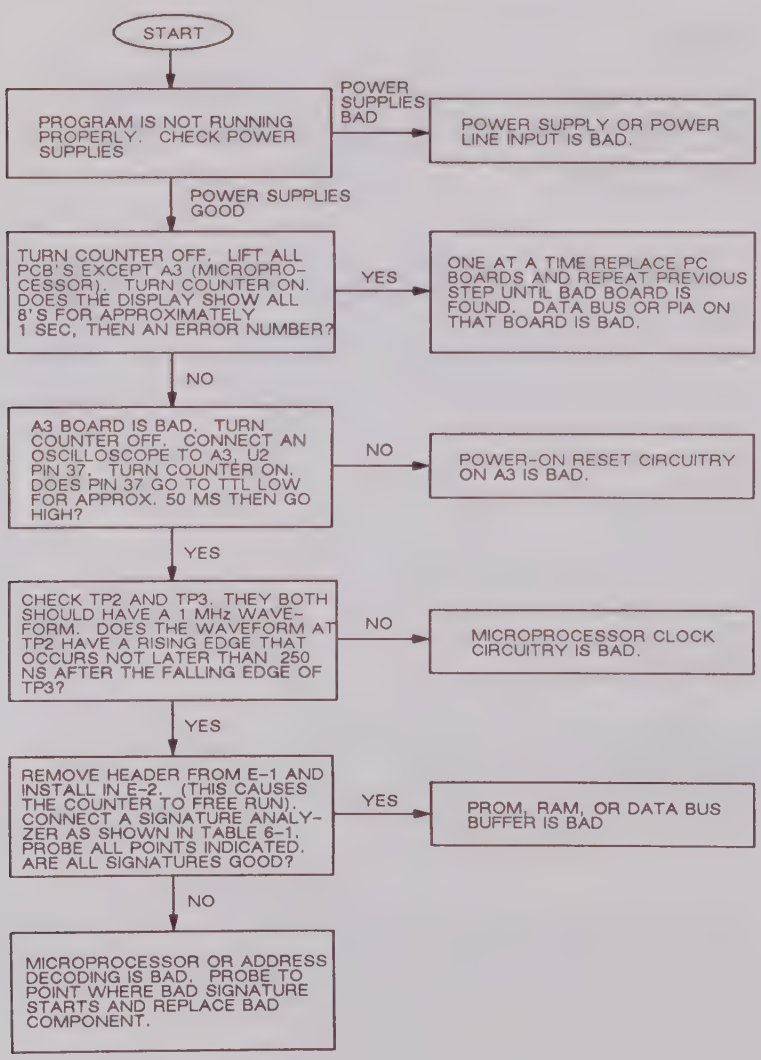

START
PROGRAM IS NOT RUNNING PROPERLY. CHECK POWER SUPPLIES
POWER SUPPLIES BAD
POWER SUPPLY OR POWER LINE INPUT IS BAD.
POWER SUPPLIES GOOD
TURN COUNTER OFF. LIFT ALL PCB'S EXCEPT A3 (MICROPROCESSOR). TURN COUNTER ON. DOES THE DISPLAY SHOW ALL 8'S FOR APPROXIMATELY 1 SEC, THEN AN ERROR NUMBER?
YES
ONE AT A TIME REPLACE PC BOARDS AND REPEAT PREVIOUS STEP UNTIL BAD BOARD IS FOUND. DATA BUS OR PIA ON THAT BOARD IS BAD.
NO
A3 BOARD IS BAD. TURN COUNTER OFF. CONNECT AN OSCILLOSCOPE TO A3, U2 PIN 37. TURN COUNTER ON. DOES PIN 37 GO TO TTL LOW FOR APPROX. 50 MS THEN GO HIGH?
NO
POWER-ON RESET CIRCUITRY ON A3 IS BAD.
YES
CHECK TP2 AND TP3. THEY BOTH SHOULD HAVE A 1 MHz WAVEFORM. DOES THE WAVEFORM AT TP2 HAVE A RISING EDGE THAT OCCURS NOT LATER THAN 250 NS AFTER THE FALLING EDGE OF TP3?
NO
MICROPROCESSOR CLOCK CIRCUITRY IS BAD.
YES
REMOVE HEADER FROM E-1 AND INSTALL IN E-2. (THIS CAUSES THE COUNTER TO FREE RUN). CONNECT A SIGNATURE ANALYZER AS SHOWN IN TABLE 6-1. PROBE ALL POINTS INDICATED. ARE ALL SIGNATURES GOOD?
YES
PROM, RAM, OR DATA BUS BUFFER IS BAD
NO
MICROPROCESSOR OR ADDRESS DECODING IS BAD. PROBE TO POINT WHERE BAD SIGNATURE STARTS AND REPLACE BAD COMPONENT.

Figure 6-2. Program Inoperative Troubleshooting Tree

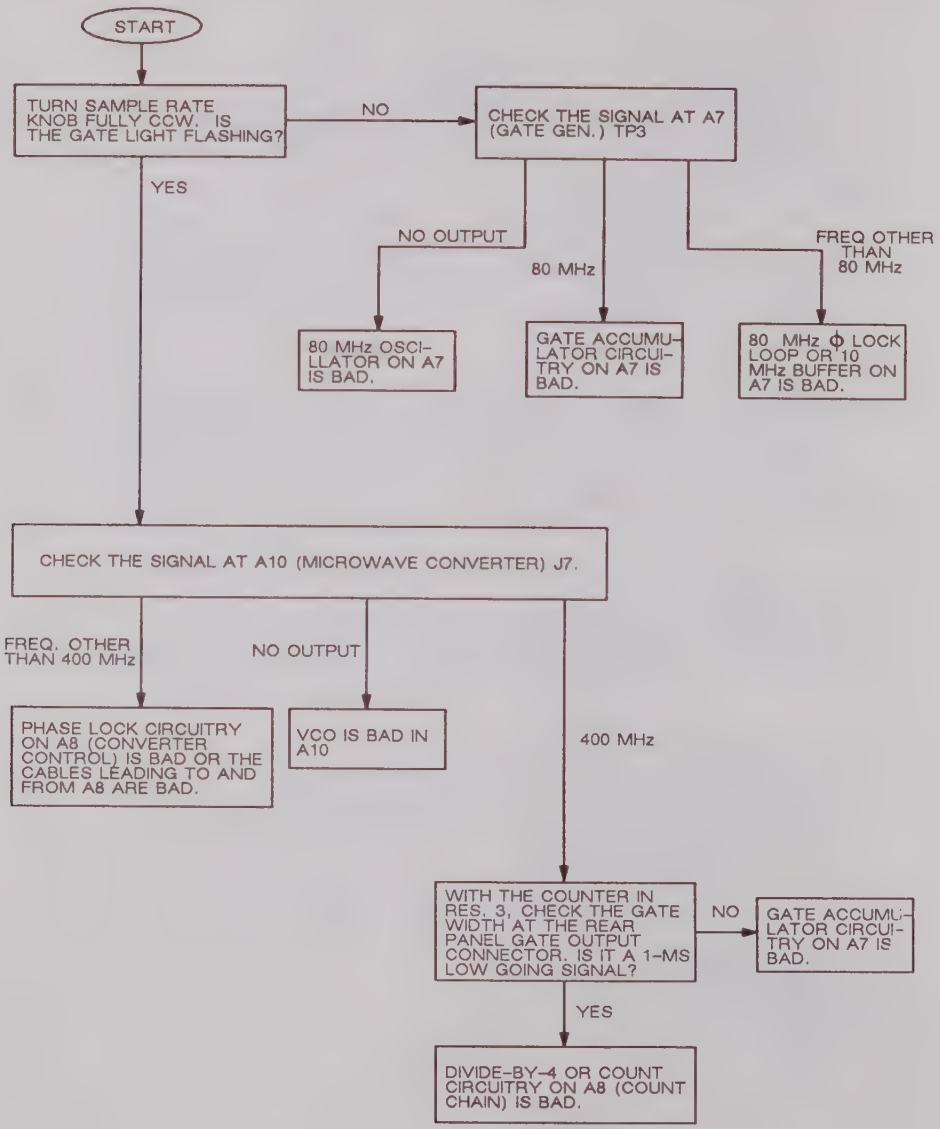

START
TURN SAMPLE RATE KNOB FULLY CCW. IS THE GATE LIGHT FLASHING?
NO
CHECK THE SIGNAL AT A7 (GATE GEN.) TP3
YES
NO OUTPUT
80 MHz
FREQ OTHER THAN 80 MHz
80 MHz OSCILLATOR ON A7 IS BAD.
GATE ACCUMULATOR CIRCUITRY ON A7 IS BAD.
80 MHz Φ LOCK LOOP OR 10 MHz BUFFER ON A7 IS BAD.
CHECK THE SIGNAL AT A10 (MICROWAVE CONVERTER) J7.
FREQ. OTHER THAN 400 MHz
NO OUTPUT
400 MHz
PHASE LOCK CIRCUITRY ON A8 (CONVERTER CONTROL) IS BAD OR THE CABLES LEADING TO AND FROM A8 ARE BAD.
VCO IS BAD IN A10
WITH THE COUNTER IN RES. 3, CHECK THE GATE WIDTH AT THE REAR PANEL GATE OUTPUT CONNECTOR. IS IT A 1-MS LOW GOING SIGNAL?
NO
GATE ACCUMULATOR CIRCUITRY ON A7 IS BAD.
YES
DIVIDE-BY-4 OR COUNT CIRCUITRY ON A8 (COUNT CHAIN) IS BAD.

Figure 6-3. 100-MHz Self Test Troubleshooting Tree

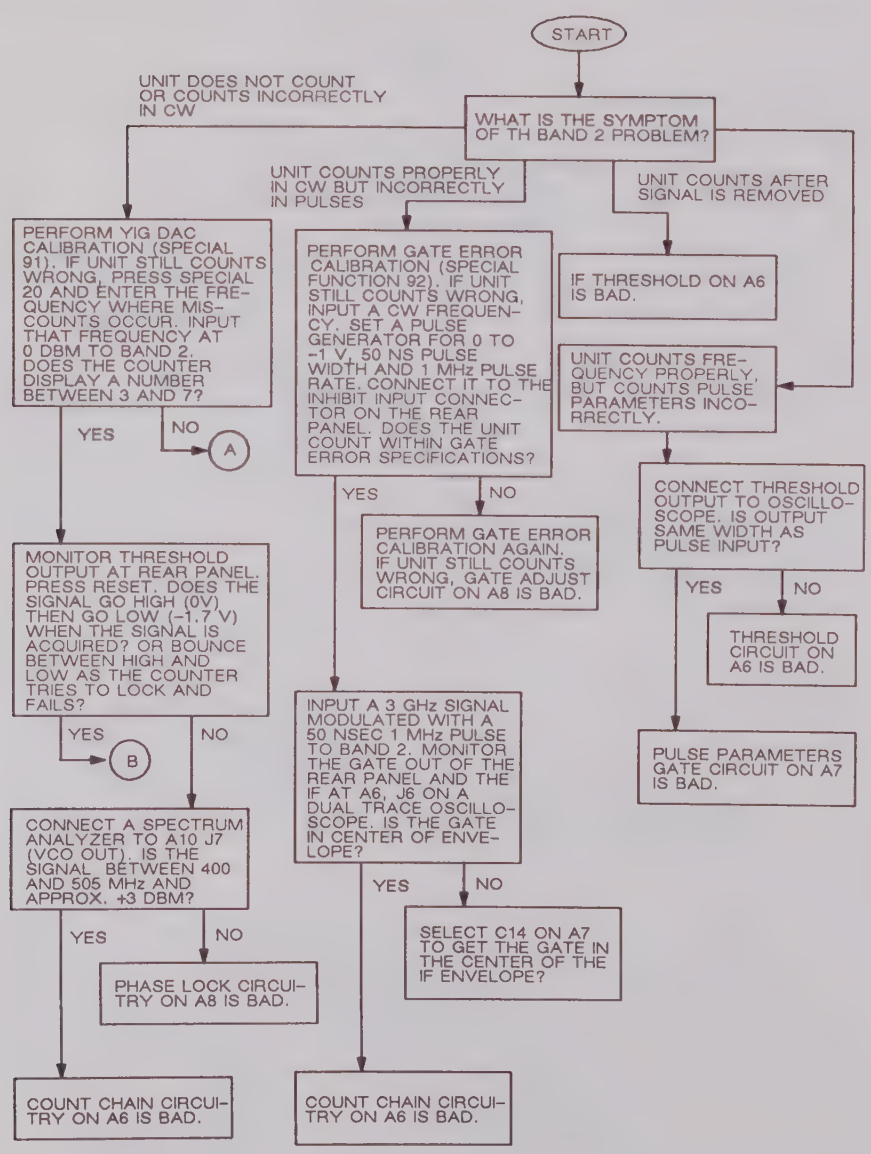

START
WHAT IS THE SYMPTOM OF TH BAND 2 PROBLEM?
UNIT DOES NOT COUNT OR COUNTS INCORRECTLY IN CW
UNIT COUNTS PROPERLY IN CW BUT INCORRECTLY IN PULSES
UNIT COUNTS AFTER SIGNAL IS REMOVED
PERFORM YIG DAC CALIBRATION (SPECIAL 91). IF UNIT STILL COUNTS WRONG, PRESS SPECIAL 20 AND ENTER THE FREQUENCY WHERE MISCOUNTS OCCUR. INPUT THAT FREQUENCY AT 0 DBM TO BAND 2. DOES THE COUNTER DISPLAY A NUMBER BETWEEN 3 AND 7?
YES
NO
A
PERFORM GATE ERROR CALIBRATION (SPECIAL FUNCTION 92). IF UNIT STILL COUNTS WRONG, INPUT A CW FREQUENCY. SET A PULSE GENERATOR FOR 0 TO -1 V, 50 NS PULSE WIDTH AND 1 MHz PULSE RATE. CONNECT IT TO THE INHIBIT INPUT CONNECTOR ON THE REAR PANEL. DOES THE UNIT COUNT WITHIN GATE ERROR SPECIFICATIONS?
YES
NO
PERFORM GATE ERROR CALIBRATION AGAIN. IF UNIT STILL COUNTS WRONG, GATE ADJUST CIRCUIT ON A8 IS BAD.
IF THRESHOLD ON A6 IS BAD.
UNIT COUNTS FREQUENCY PROPERLY, BUT COUNTS PULSE PARAMETERS INCORRECTLY.
CONNECT THRESHOLD OUTPUT TO OSCILLOSCOPE. IS OUTPUT SAME WIDTH AS PULSE INPUT?
YES
NO
THRESHOLD CIRCUIT ON A6 IS BAD.
PULSE PARAMETERS GATE CIRCUIT ON A7 IS BAD.
MONITOR THRESHOLD OUTPUT AT REAR PANEL. PRESS RESET. DOES THE SIGNAL GO HIGH (0V) THEN GO LOW (-1.7 V) WHEN THE SIGNAL IS ACQUIRED? OR BOUNCE BETWEEN HIGH AND LOW AS THE COUNTER TRIES TO LOCK AND FAILS?
YES
NO
B
INPUT A 3 GHz SIGNAL MODULATED WITH A 50 NSEC 1 MHz PULSE TO BAND 2. MONITOR THE GATE OUT OF THE REAR PANEL AND THE IF AT A6, J6 ON A DUAL TRACE OSCILLOSCOPE. IS THE GATE IN CENTER OF ENVELOPE?
YES
NO
SELECT C14 ON A7 TO GET THE GATE IN THE CENTER OF THE IF ENVELOPE?
CONNECT A SPECTRUM ANALYZER TO A10 J7 (VCO OUT). IS THE SIGNAL BETWEEN 400 AND 505 MHz AND APPROX. +3 DBM?
YES
NO
PHASE LOCK CIRCUITRY ON A8 IS BAD.
COUNT CHAIN CIRCUITRY ON A6 IS BAD.
COUNT CHAIN CIRCUITRY ON A6 IS BAD.

Figure 6-4. Band 2 Troubleshooting Tree

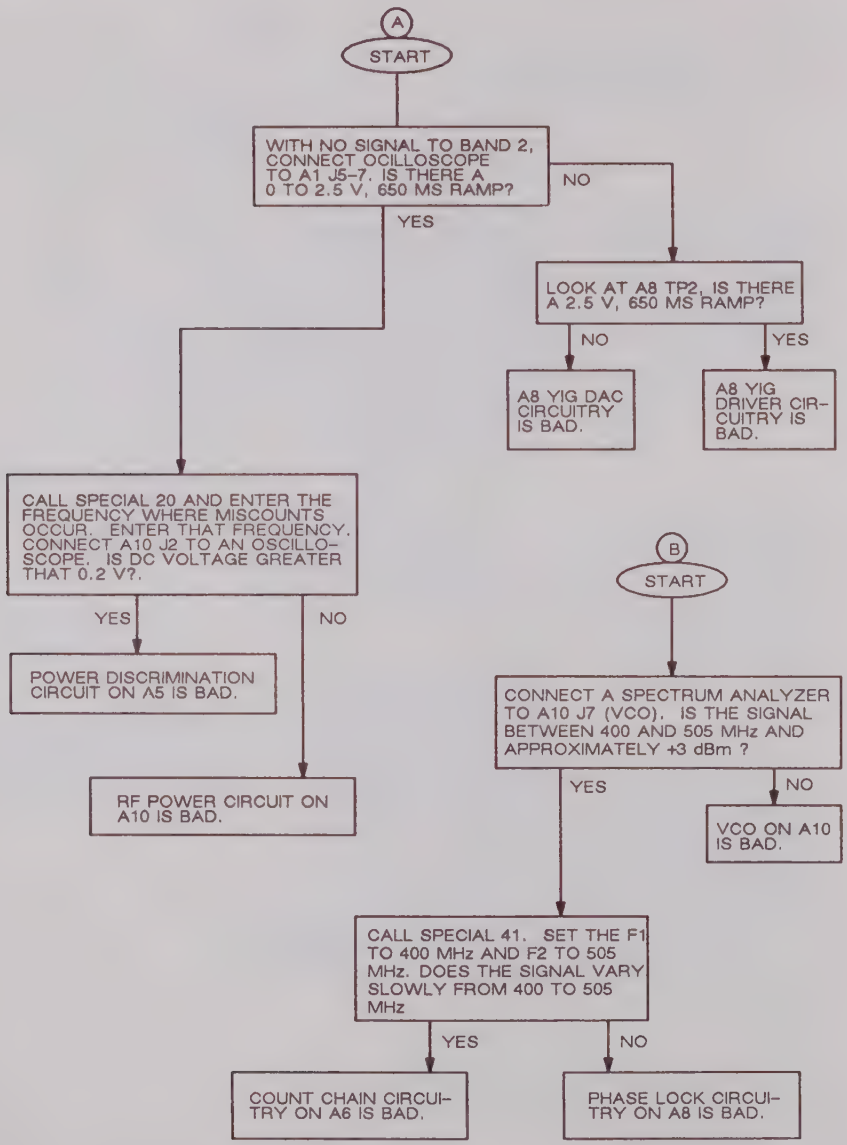

A
START
WITH NO SIGNAL TO BAND 2, CONNECT OCILLOSCOPE TO A1 J5-7. IS THERE A 0 TO 2.5 V, 650 MS RAMP?
NO
YES
LOOK AT A8 TP2, IS THERE A 2.5 V, 650 MS RAMP?
NO
YES
A8 YIG DAC CIRCUITRY IS BAD.
A8 YIG DRIVER CIR-CUITRY IS BAD.
CALL SPECIAL 20 AND ENTER THE FREQUENCY WHERE MISCOUNTS OCCUR. ENTER THAT FREQUENCY. CONNECT A10 J2 TO AN OSCILLO-SCOPE. IS DC VOLTAGE GREATER THAT 0.2 V?.
YES
NO
POWER DISCRIMINATION CIRCUIT ON A5 IS BAD.
RF POWER CIRCUIT ON A10 IS BAD.
B
START
CONNECT A SPECTRUM ANALYZER TO A10 J7 (VCO). IS THE SIGNAL BETWEEN 400 AND 505 MHz AND APPROXIMATELY +3 dBm ?
YES
NO
VCO ON A10 IS BAD.
CALL SPECIAL 41. SET THE F1 TO 400 MHz AND F2 TO 505 MHz. DOES THE SIGNAL VARY SLOWLY FROM 400 TO 505 MHz
YES
NO
COUNT CHAIN CIRCUI-TRY ON A6 IS BAD.
PHASE LOCK CIRCUI-TRY ON A8 IS BAD.

Figure 6-4. Band 2 Troubleshooting Tree, continued

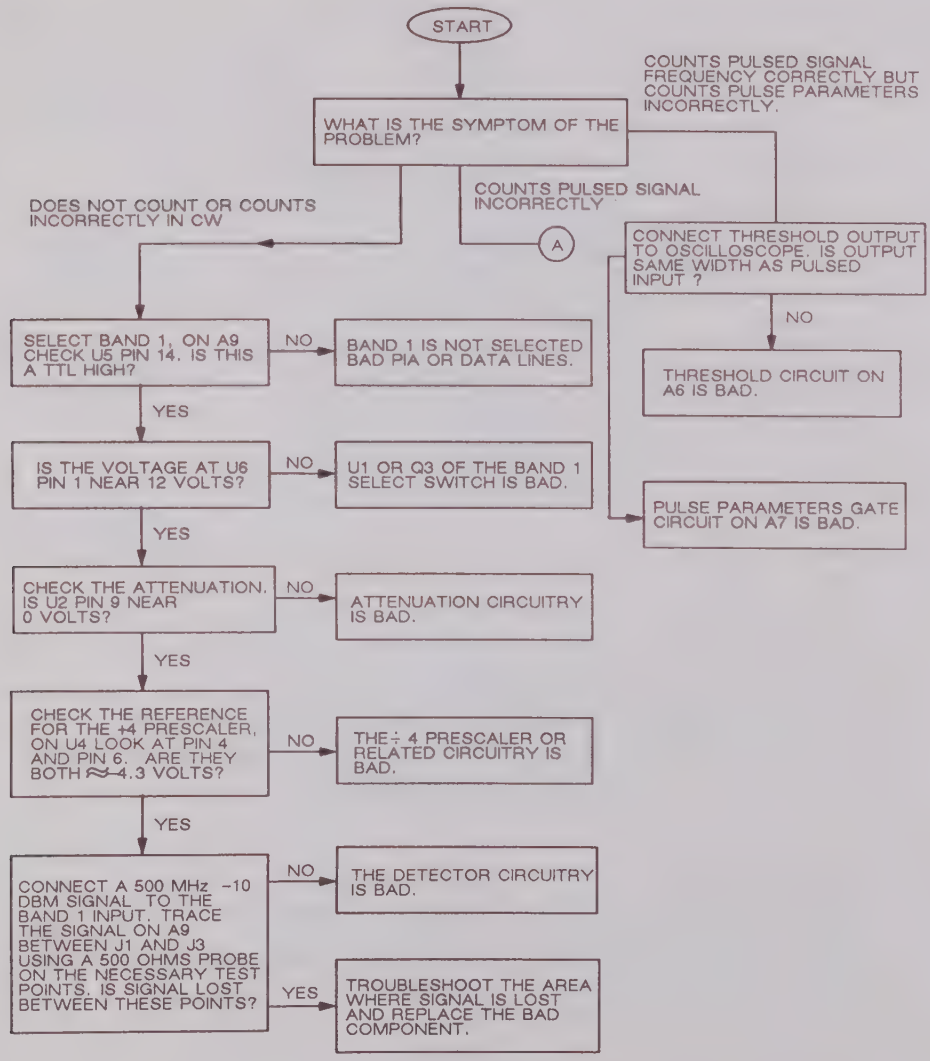

START
WHAT IS THE SYMPTOM OF THE PROBLEM?
COUNTS PULSED SIGNAL FREQUENCY CORRECTLY BUT COUNTS PULSE PARAMETERS INCORRECTLY.
COUNTS PULSED SIGNAL INCORRECTLY
DOES NOT COUNT OR COUNTS INCORRECTLY IN CW
A
CONNECT THRESHOLD OUTPUT TO OSCILLOSCOPE. IS OUTPUT SAME WIDTH AS PULSED INPUT ?
NO
THRESHOLD CIRCUIT ON A6 IS BAD.
SELECT BAND 1, ON A9 CHECK U5 PIN 14. IS THIS A TTL HIGH?
NO
BAND 1 IS NOT SELECTED BAD PIA OR DATA LINES.
YES
IS THE VOLTAGE AT U6 PIN 1 NEAR 12 VOLTS?
NO
U1 OR Q3 OF THE BAND 1 SELECT SWITCH IS BAD.
YES
PULSE PARAMETERS GATE CIRCUIT ON A7 IS BAD.
CHECK THE ATTENUATION. IS U2 PIN 9 NEAR 0 VOLTS?
NO
ATTENUATION CIRCUITRY IS BAD.
YES
CHECK THE REFERENCE FOR THE ÷4 PRESCALER, ON U4 LOOK AT PIN 4 AND PIN 6. ARE THEY BOTH ≈4.3 VOLTS?
NO
THE ÷ 4 PRESCALER OR RELATED CIRCUITRY IS BAD.
YES
CONNECT A 500 MHz −10 DBM SIGNAL TO THE BAND 1 INPUT. TRACE THE SIGNAL ON A9 BETWEEN J1 AND J3 USING A 500 OHMS PROBE ON THE NECESSARY TEST POINTS. IS SIGNAL LOST BETWEEN THESE POINTS?
NO
THE DETECTOR CIRCUITRY IS BAD.
YES
TROUBLESHOOT THE AREA WHERE SIGNAL IS LOST AND REPLACE THE BAD COMPONENT.

Figure 6-5. Band 1 Troubleshooting Tree (Option)

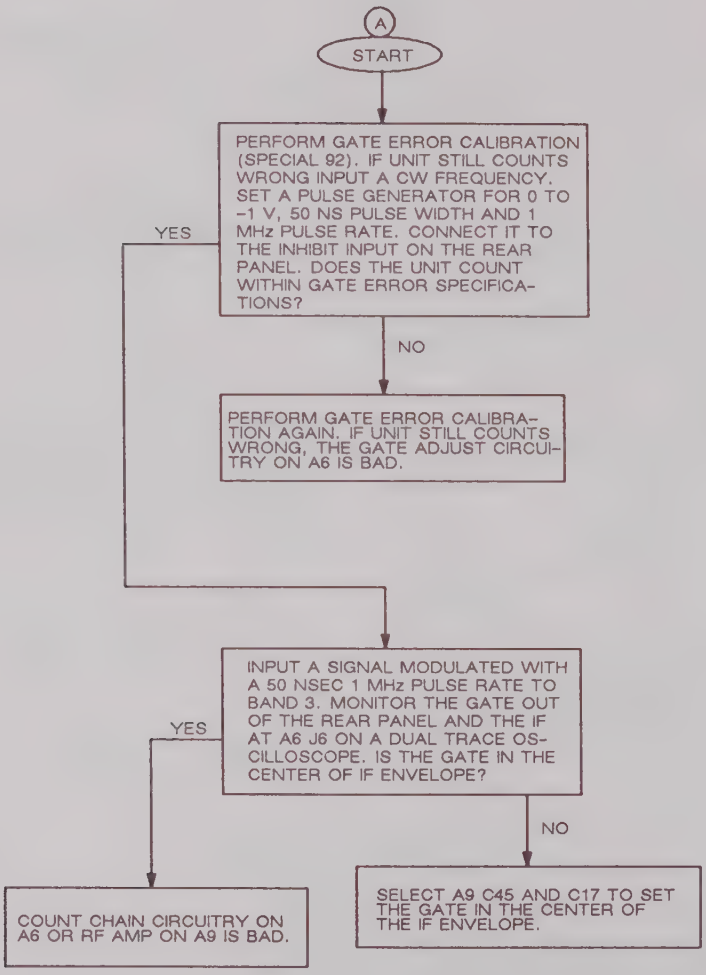

A
START
PERFORM GATE ERROR CALIBRATION (SPECIAL 92). IF UNIT STILL COUNTS WRONG INPUT A CW FREQUENCY. SET A PULSE GENERATOR FOR 0 TO -1 V, 50 NS PULSE WIDTH AND 1 MHz PULSE RATE. CONNECT IT TO THE INHIBIT INPUT ON THE REAR PANEL. DOES THE UNIT COUNT WITHIN GATE ERROR SPECIFICATIONS?
YES
NO
PERFORM GATE ERROR CALIBRATION AGAIN. IF UNIT STILL COUNTS WRONG, THE GATE ADJUST CIRCUITRY ON A6 IS BAD.
INPUT A SIGNAL MODULATED WITH A 50 NSEC 1 MHz PULSE RATE TO BAND 3. MONITOR THE GATE OUT OF THE REAR PANEL AND THE IF AT A6 J6 ON A DUAL TRACE OSCILLOSCOPE. IS THE GATE IN THE CENTER OF IF ENVELOPE?
YES
NO
COUNT CHAIN CIRCUITRY ON A6 OR RF AMP ON A9 IS BAD.
SELECT A9 C45 AND C17 TO SET THE GATE IN THE CENTER OF THE IF ENVELOPE.

Figure 6-5. Band 1 Troubleshooting Tree (Option), continued

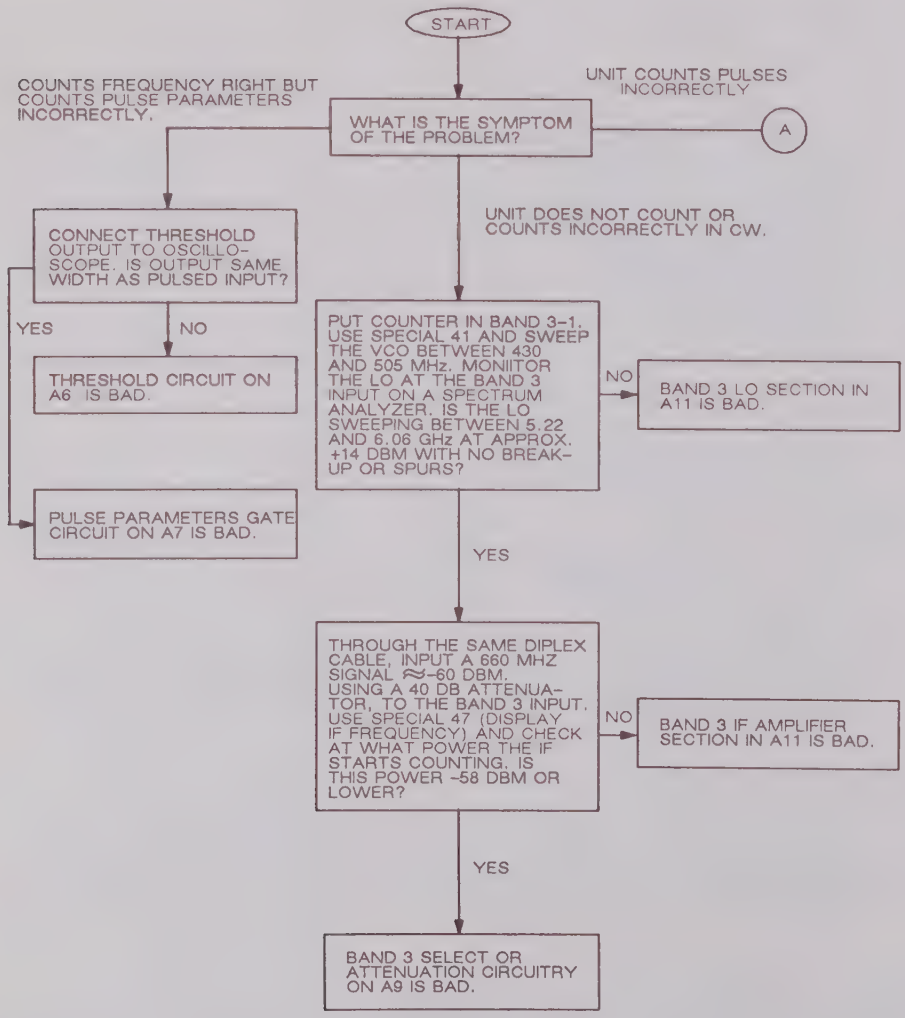

START
COUNTS FREQUENCY RIGHT BUT COUNTS PULSE PARAMETERS INCORRECTLY.
WHAT IS THE SYMPTOM OF THE PROBLEM?
UNIT COUNTS PULSES INCORRECTLY
A
UNIT DOES NOT COUNT OR COUNTS INCORRECTLY IN CW.
CONNECT THRESHOLD OUTPUT TO OSCILLO-SCOPE. IS OUTPUT SAME WIDTH AS PULSED INPUT?
YES
NO
THRESHOLD CIRCUIT ON A6 IS BAD.
PULSE PARAMETERS GATE CIRCUIT ON A7 IS BAD.
PUT COUNTER IN BAND 3-1. USE SPECIAL 41 AND SWEEP THE VCO BETWEEN 430 AND 505 MHz. MONITOR THE LO AT THE BAND 3 INPUT ON A SPECTRUM ANALYZER. IS THE LO SWEEPING BETWEEN 5.22 AND 6.06 GHz AT APPROX. +14 DBM WITH NO BREAK-UP OR SPURS?
NO
BAND 3 LO SECTION IN A11 IS BAD.
YES
THROUGH THE SAME DIPLEX CABLE, INPUT A 660 MHZ SIGNAL ≈-60 DBM. USING A 40 DB ATTENUA-TOR, TO THE BAND 3 INPUT. USE SPECIAL 47 (DISPLAY IF FREQUENCY) AND CHECK AT WHAT POWER THE IF STARTS COUNTING. IS THIS POWER -58 DBM OR LOWER?
NO
BAND 3 IF AMPLIFIER SECTION IN A11 IS BAD.
YES
BAND 3 SELECT OR ATTENUATION CIRCUITRY ON A9 IS BAD.

Figure 6-6. Band 3 Troubleshooting Tree (Option)

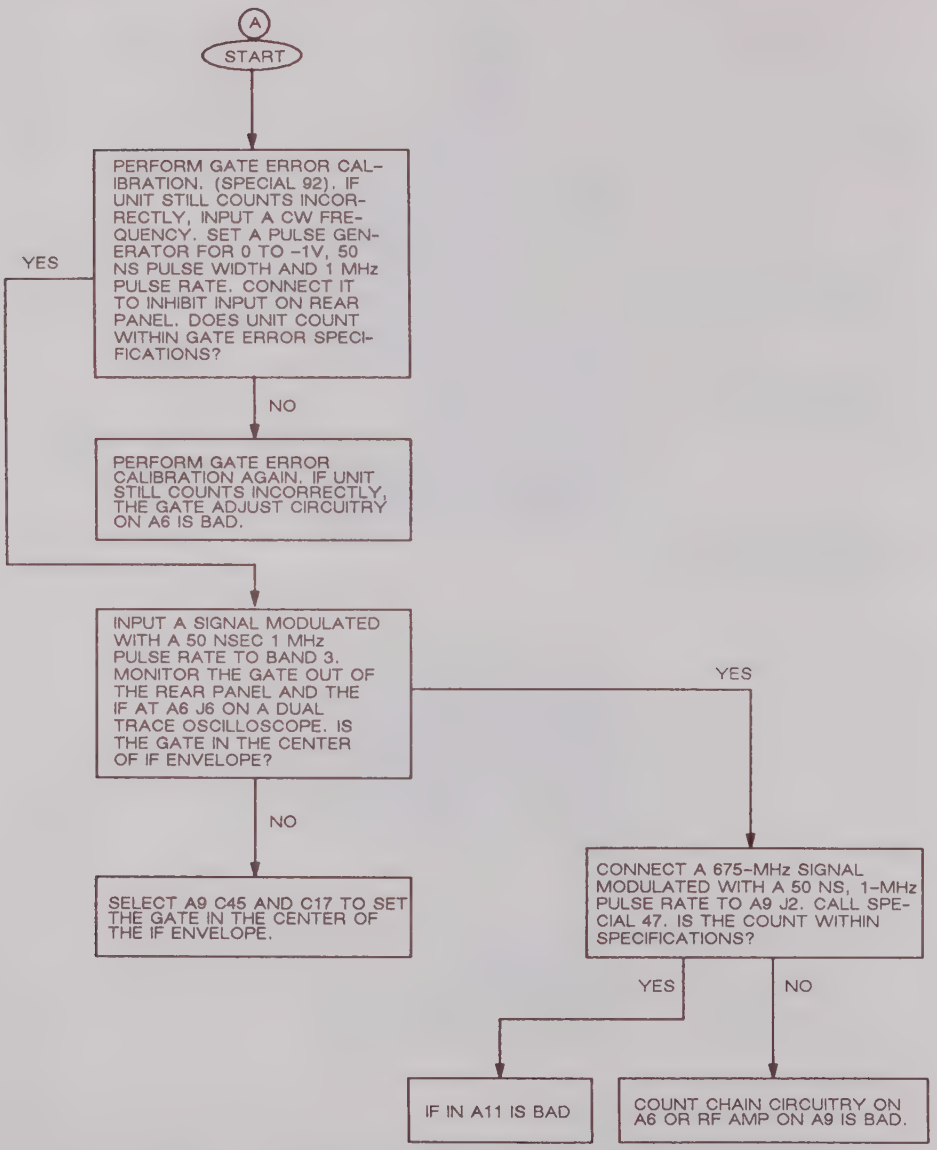

A
START
PERFORM GATE ERROR CALIBRATION. (SPECIAL 92). IF UNIT STILL COUNTS INCORRECTLY, INPUT A CW FREQUENCY. SET A PULSE GENERATOR FOR 0 TO -1V, 50 NS PULSE WIDTH AND 1 MHz PULSE RATE. CONNECT IT TO INHIBIT INPUT ON REAR PANEL. DOES UNIT COUNT WITHIN GATE ERROR SPECIFICATIONS?
YES
NO
PERFORM GATE ERROR CALIBRATION AGAIN. IF UNIT STILL COUNTS INCORRECTLY, THE GATE ADJUST CIRCUITRY ON A6 IS BAD.
INPUT A SIGNAL MODULATED WITH A 50 NSEC 1 MHz PULSE RATE TO BAND 3. MONITOR THE GATE OUT OF THE REAR PANEL AND THE IF AT A6 J6 ON A DUAL TRACE OSCILLOSCOPE. IS THE GATE IN THE CENTER OF IF ENVELOPE?
YES
NO
SELECT A9 C45 AND C17 TO SET THE GATE IN THE CENTER OF THE IF ENVELOPE.
CONNECT A 675-MHz SIGNAL MODULATED WITH A 50 NS, 1-MHz PULSE RATE TO A9 J2. CALL SPECIAL 47. IS THE COUNT WITHIN SPECIFICATIONS?
YES
NO
IF IN A11 IS BAD
COUNT CHAIN CIRCUITRY ON A6 OR RF AMP ON A9 IS BAD.

Figure 6-6. Band 3 Troubleshooting Tree (Option), continued

# Section 7
# Theory of Operation

## INTRODUCTION

The Models 585 and 588 microwave pulsed counters are microprocessor-based multifunction instruments. These counters are able to measure CW and pulsed signals automatically with pulse widths as narrow as 50 ns and pulse periods as high as 250 ns. These counters also measure the pulse width or pulse period of the input signal to a 15-ns resolution. Through the inhibit input, the instruments can profile pulsed or chirped CW signals with gates as narrow as 15 ns. No manual switching is required to measure CW or pulsed signals. A block diagram of the 585/588 counter is shown in Figure 7-1.

The frequency range of the 585 is 0.95 GHz to 18 GHz, and can be extended by option down to 300 MHz. The frequency range of the 588 is 0.95 GHz to 26.5 GHz, and can be extended by option down to 300 MHz and up to 110 GHz. On both instruments the range of the pulse parameter measurements is 10 ns (when profiling) to 9.99 seconds.

All major functions are controlled through the 21-button, functionally grouped keyboard. Information is output via a 9-digit sectionalized LED frequency display, a 3-digit floating point LED pulse parameter display, and a 20-message LED annunciator bank.

Microprocessor control and the unique architecture permit not only the major counter functions such as frequency offsets, frequency range limits, and averaging capabilities, but also a variety of special functions such as internal diagnostics, calibration and test aids, and sophisticated operational enhancements.

All front panel controls except the ON/OFF switch, and all background functions are externally programmable via the IEEE 488-1978 standard GPIB (General Purpose Interface Bus) port. Additionally all displayed information, as well as instrument setup status, is accessible via the GPIB.

The instrument can best be understood by considering the three major sections: the basic counter, the microwave converter, and the optional millimeter/RF converters.

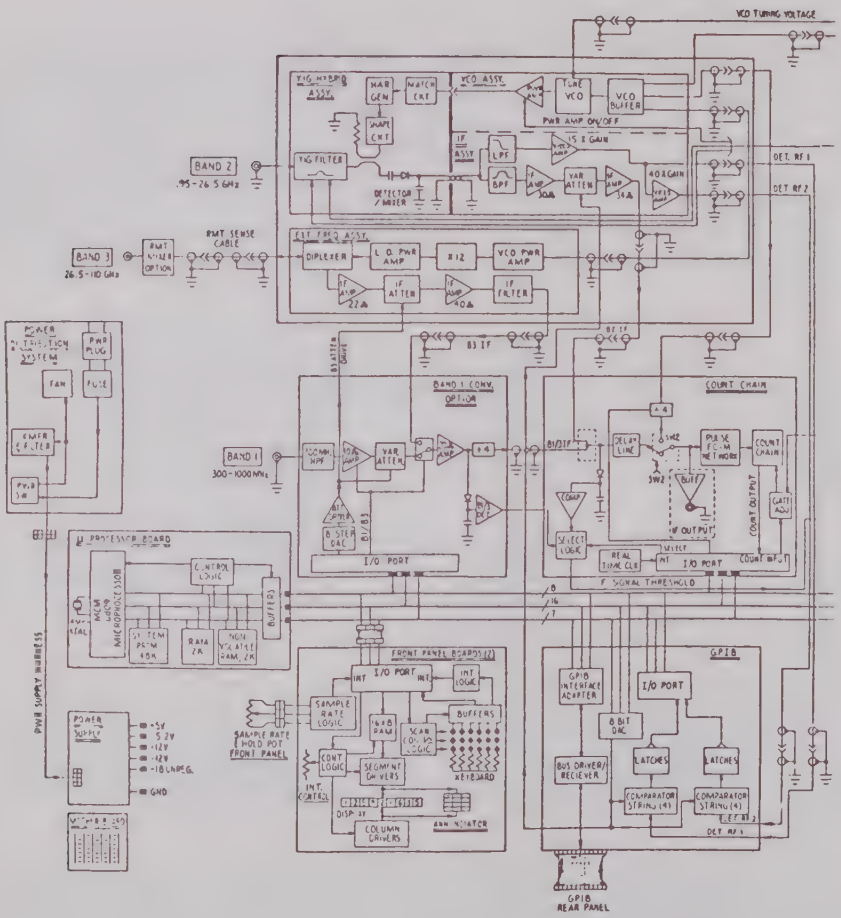



Figure 7-1. Block Diagram of 585/588 Counters

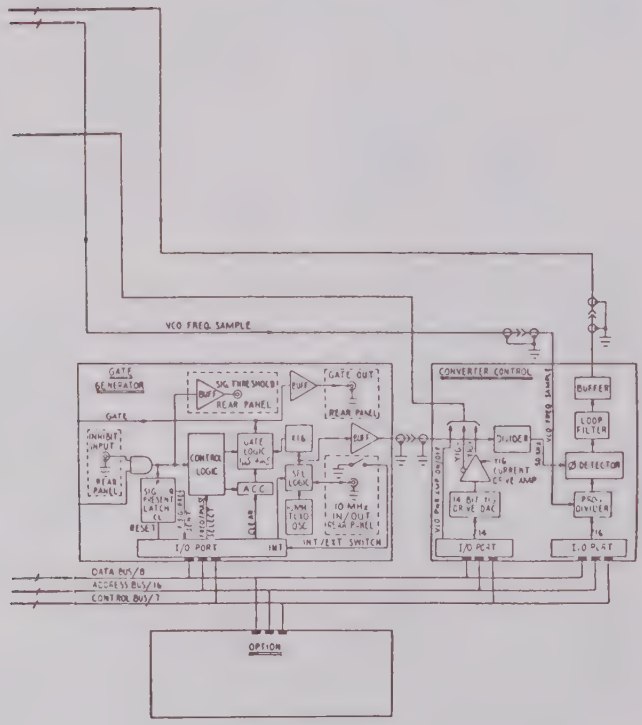



Figure 7-1. Block Diagram of 585/588 Counters (cont.)

## BASIC COUNTER

The basic counter accepts the IF signal from either the microwave converter or the millimeter/RF converters and measures the frequency, pulse width, or pulse period of the IF. A block diagram of the basic counter is shown in Figure 7-2.

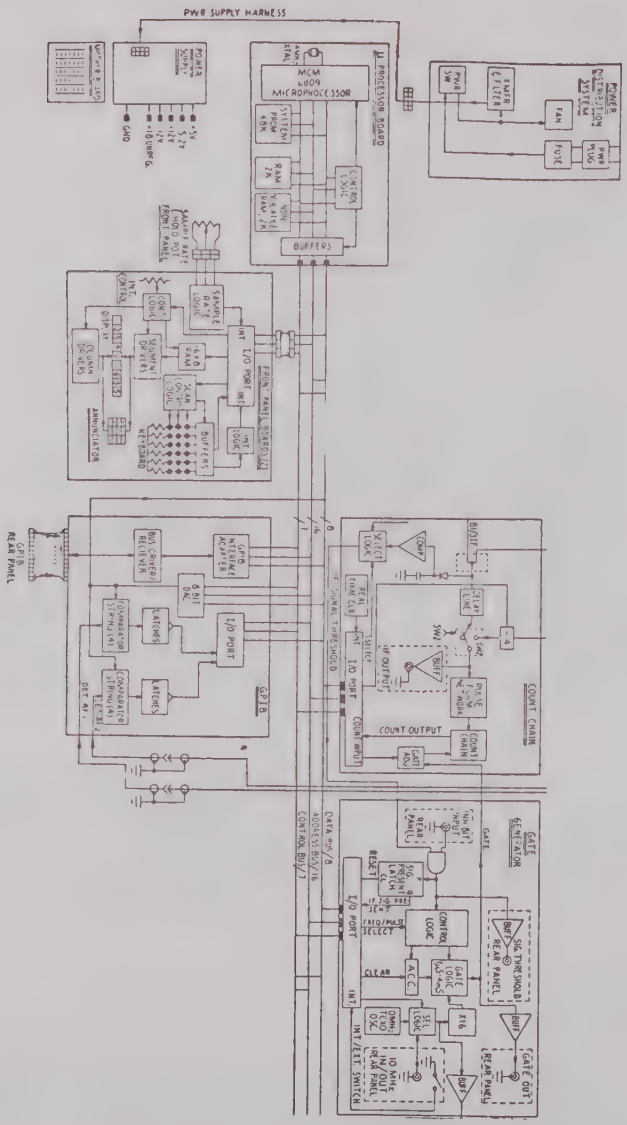



Figure 7-2. Block Diagram of Basic Counter.

Overall operation is controlled by the microprocessor assembly, A3. This assembly contains a Motorola 6809 microprocessor, its control logic, and the system memory. It communicates with all other assemblies in the instrument by means of a triple bus system: the data bus, address bus, and control bus. On each assembly there is a peripheral interface adapter (PIA) that provides the interface between the bus system and the instrument hardware.

Frequency measurements are performed by comparing an unknown signal to a reference frequency, namely the time base. A 10 MHz temperature compensated crystal oscillator (TCXO) is used as the internal reference. For coherence with system clocks, the user may select an external 10 MHz reference.

A frequency measurement is made by generating a time interval (gate time) consisting of a number of cycles of the reference. This gate time is used as an interval during which the input signal is counted by the count chain assembly. This function is considerably more difficult for pulsed signals than it is for CW signals and must be accomplished as two functions. The first is to supply a gate to the count chain that is present only when an input signal is also present. The second is to accumulate the total time during which the gate is applied until the desired gate time is reached.

The first operation requires that the gate begin after the signal is present at the count chain and end prior to the end of the signal. This is accomplished by generating a gate approximately 30 nanoseconds shorter than the RF signal. The arrival time at the count chain of the IF from the converter is then controlled by a delay line so the gate will fall entirely within the IF pulse.

The second operation is accomplished by counting reference clock pulses whenever the gate is open until a total time equal to 1/resolution is obtained. This requires that each gate opening is an exact integral number of clock pulses. An 80-MHz clock is used for this, causing the gate to be an exact multiple of 12.5 nanoseconds.

Pulse width is measured by counting a known frequency for the time the signal is present. Pulse period is measured by counting a known frequency for the time between the start of one pulse and the start of the next. The known frequency is the 400-500 MHz VCO prescaled by four.

## BAND 2 MICROWAVE CONVERTER

Measurement of a signal in the microwave band is accomplished by down converting from the microwave range to approximately 110 MHz. This is accomplished by mixing the input signal with a known reference frequency that is a harmonic of the VCO. The VCO frequency (400-500 MHz) can be selected in 50 kHz increments by using a microprocessor-controlled phase lock system while retaining the accuracy and stability of the counter's time base reference.

A simplified diagram of the microwave converter is shown in Figure 7-3. There are two major assemblies, the Converter Control assembly and the Converter assembly.

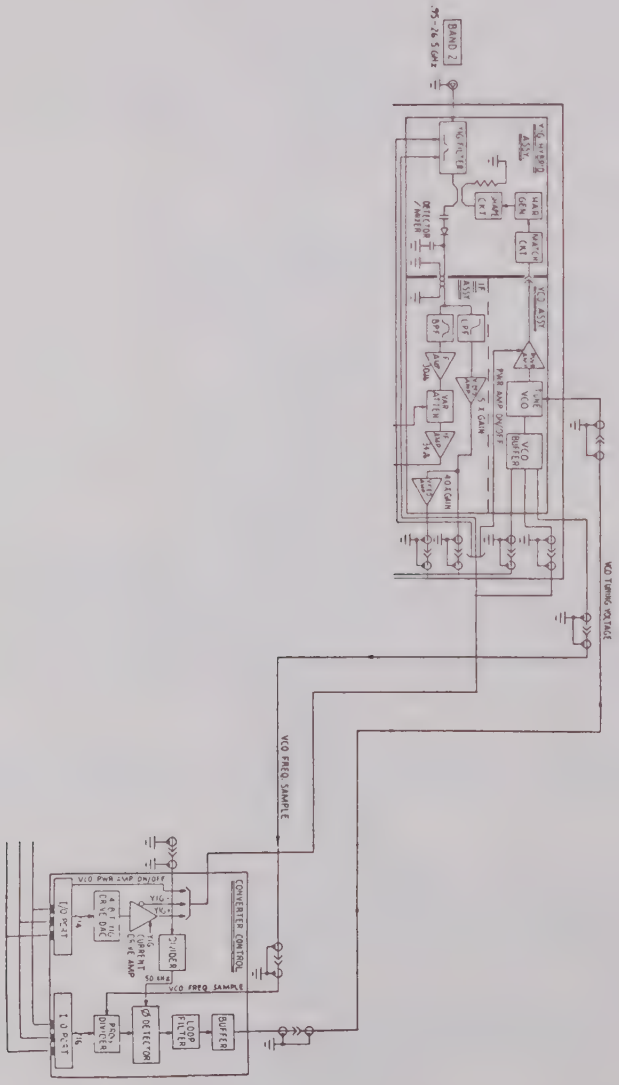



Figure 7-3. Block Diagram, Microwave Converter

## CONVERTER CONTROL

The Converter Control assembly contains the interface between the microprocessor bus system and the Converter. A digital-to-analog converter and a precision current driver provide a 2-MHz frequency resolution for setting the YIG filter of the Microwave assembly.

The Converter Control also contains the programmable VCO phase lock control system. This system lets the microprocessor select any VCO frequency between 400 and 500 MHz, in increments of 50 kHz.

## CONVERTER

The Converter assembly consists of three subassemblies.

- Voltage Controlled Oscillator (VCO) assembly
- IF Amplifier assembly
- Microwave assembly (YIG)

The Microwave assembly contains the YIG filter, mixer, and comb generator.

The input signal (0.95 GHz to 18 GHz/26.5 GHz) passes through a YIG filter. The filter is an electronically tunable bandpass filter with an operating frequency proportional to its tuning current. This filter determines the approximate frequency of the input signal and filters out any undesired signals, making it possible to count a signal at one frequency even if a larger signal is present at another frequency.

When the YIG filter is being tuned to the input signal, the mixer is used as an RF detector, and its output is amplified in the video amplifier on the IF assembly.

The output of the video amplifier is maximum when the YIG filter is tuned to the input signal. In the case of multiple input signals, the video amplifier output determines which signal is largest.

Once the YIG filter is tuned to the input signal, the appropriate harmonic number (N) and VCO frequency ($F_{VCO}$) are selected to produce an IF frequency ($F_{IF}$) at approximately 110 MHz. The input signal is found by using:

$$F_{IN} = N \times F_{VCO} \pm F_{IF}$$

The IF frequency produced in the mixer is amplified by the high-gain IF amplifier and sent to the count chain.

## OPERATION

See Figure 7-4 for a simplified diagram of microwave converter operation.

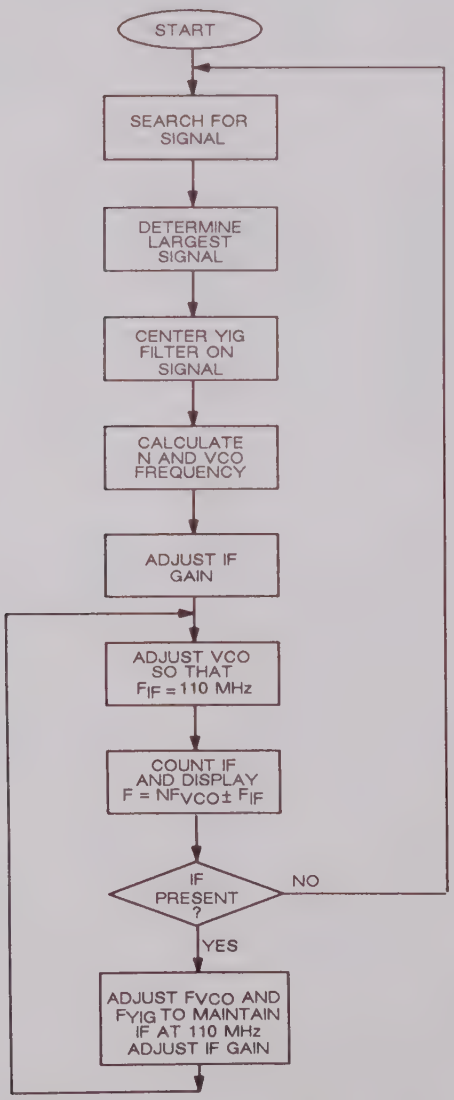

START
SEARCH FOR SIGNAL
DETERMINE LARGEST SIGNAL
CENTER YIG FILTER ON SIGNAL
CALCULATE N AND VCO FREQUENCY
ADJUST IF GAIN
ADJUST VCO SO THAT $F_{IF}$ = 110 MHz
COUNT IF AND DISPLAY $F = NF_{VCO} \pm F_{IF}$
IF PRESENT ?
NO
YES
ADJUST FVCO AND FYIG TO MAINTAIN IF AT 110 MHz ADJUST IF GAIN

Figure 7-4. Flow Diagram Microwave Converter Operation

First the YIG filter is stepped from its low to high limits. During this search, the RF detected output is fed to a series of detectors set 4.5 dB apart. After each step, the threshold detectors are checked. If the detectors are triggered, the approximate amplitude of the signal is remembered by the microprocessor. The counter then returns to the search mode to look for any larger signals. After searching the entire frequency range, it returns to the largest signal and begins to center the YIG filter precisely on the input frequency.

The centering process consists of finding the exact relative power of the signal, then stepping the YIG in 2-MHz steps until four points are found: the points on either side of the peak 1.5 dB down from the peak, and the points on either side of the peak 4.5 dB down from the peak. From these points the approximate "center of mass frequency" of the signal is found and the YIG filter set to that frequency. The "center of mass" algorithm compensates for pulsed signals that deviate from a perfect sinX / X shape, and for non-symmetries in the YIG filter.

After the signal is centered, N is determined from

$$\frac{F_{YIG} - 110}{500}$$

and then rounded up to the next higher integer. From this, $F_{VCO}$ is calculated using

$$F_{VCO} = \frac{F_{YIG} - 110}{N}$$

Should this yield $F_{VCO} = <400$ MHz, then $F_{VCO}$ is recalculated using

$$F_{VCO} = \frac{F_{YIG} + 110}{N}$$

After the IF is found, the IF gain is adjusted to set the signal threshold approximately 3 dB below the peak amplitude.

Since $F_{YIG}$ is only approximately equal to $F_{IN}$, the IF frequency will not be exactly 110 MHz. Therefore, the next step in the operation is a VCO frequency adjustment to shift $F_{IF}$ into the middle of the IF passband.

VCO frequency correction is achieved by counting $F_{IF}$ and changing $F_{VCO}$ by

$$\frac{\pm F_{IF} - 110}{N}$$

Once the VCO corrections have been made, the converter has acquired the signal and the counter counts and displays the input frequency.

After each measurement, new frequencies for the YIG and VCO are calculated to maintain the IF at 110 MHz and the IF gain is re-adjusted to keep the signal 3 dB above threshold. This method provides rapid tracking of a signal being tuned.

## MILLIMETER/RF CONVERTERS

A block diagram of the millimeter/RF converters is shown in Figure 7-5.

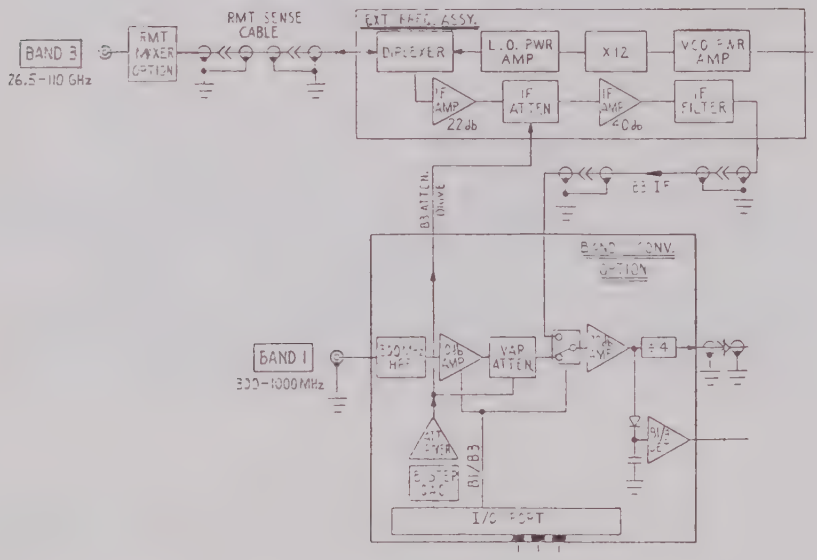



Figure 7-5. Millimeter/RF Converters

## BAND 3 MILLIMETER WAVE CONVERTER

When the 588 measures a signal frequency greater than 26.5 GHz, using a Model 890 cable and a remote sensor, it converts the signal to approximately 675 MHz, where it is directly counted by the RF converter. The VCO signal, used in this band between 435 and 505 MHz, is multiplied by 12 to the 5.22-6.06 GHz range. This signal provides the LO power which is transmitted through a diplexer to the remote sensor. The remote sensor is a harmonic mixer that generates harmonics of the LO. One of these harmonics mixes with the input to provide an IF at 675 MHz. The IF returns on the same line as the LO, is amplified by a variable gain amplifier to approximately -5 dBm, and is counted by the RF converter. See Figure 7-7, Millimeter Wave Converter Lock Process.

Initially the instrument determines the sweep range limits of the LO based on the entered sub-band. The higher the sub-band number, the smaller the LO sweep range. Then the LO is swept between its sweep limits and searches for a signal.

When a signal is found, the LO is stepped a small amount and, depending on the direction of the IF step, the mix side is found. If the instrument is in the normal mode, it determines the LO harmonic number using an eight-point algorithm that determines the harmonic number from the ratio of the IF step to the LO step. If the instrument is in the center frequency mode, the harmonic number is calculated based on the entered center frequency. The LO is then adjusted to set the IF to approximately 675 MHz. After each LO step, the IF gain is adjusted to set the detector threshold 3 dB below the peak amplitude.

The IF is measured and the frequency calculated and displayed using the formula:

$$FREQ = N \times (LO) \pm IF$$

After each measurement, the IF frequency is re-adjusted to 675 MHz and the IF gain is re-adjusted to set the peak 3 dB above threshold.

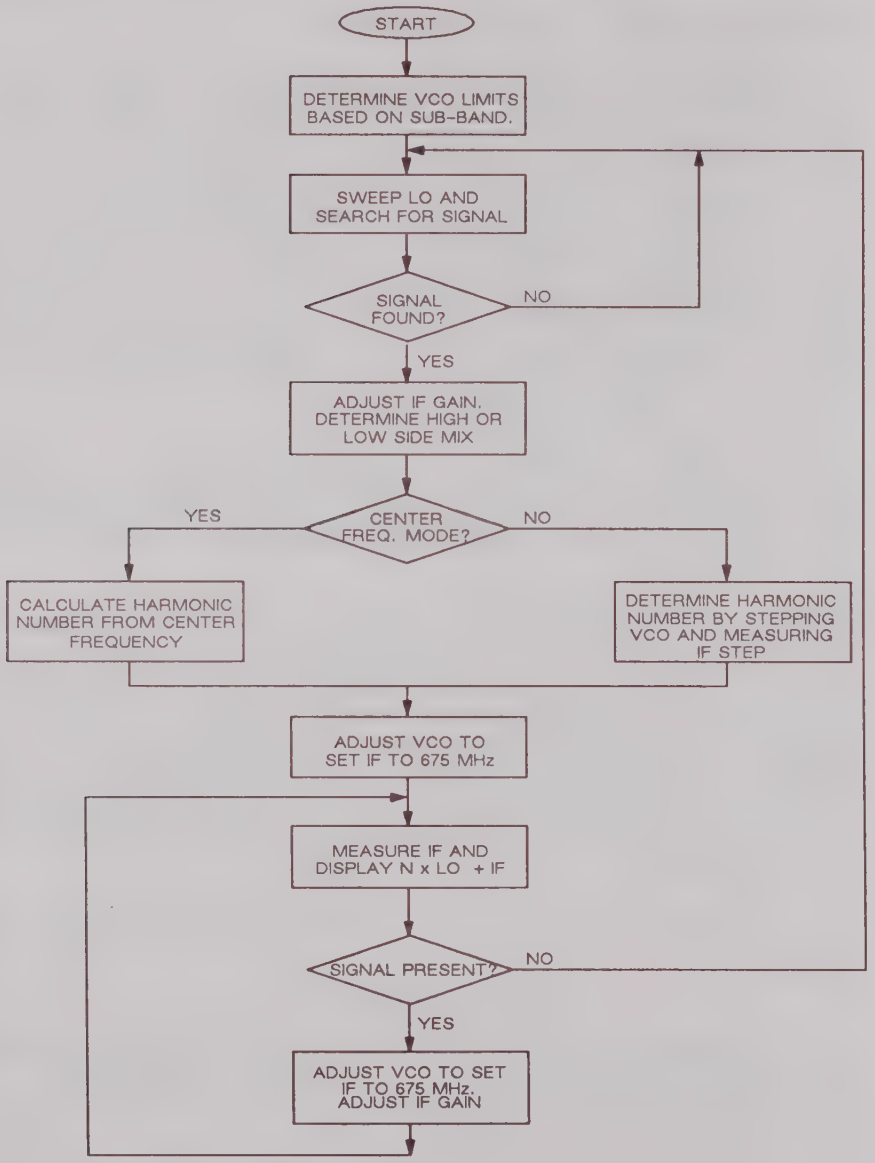

START
DETERMINE VCO LIMITS BASED ON SUB-BAND.
SWEEP LO AND SEARCH FOR SIGNAL
SIGNAL FOUND?
NO
YES
ADJUST IF GAIN. DETERMINE HIGH OR LOW SIDE MIX
CENTER FREQ. MODE?
YES
NO
CALCULATE HARMONIC NUMBER FROM CENTER FREQUENCY
DETERMINE HARMONIC NUMBER BY STEPPING VCO AND MEASURING IF STEP
ADJUST VCO TO SET IF TO 675 MHz
MEASURE IF AND DISPLAY N x LO + IF
SIGNAL PRESENT?
NO
YES
ADJUST VCO TO SET IF TO 675 MHz. ADJUST IF GAIN

Figure 7-6. Flow Diagram Millimeter Wave Converter Lock Process

## BAND 1 RF CONVERTER

Signals between 300 MHz and 1 GHz are counted directly through a divide-by-four prescaler. In this mode, the gate must be made four times longer to properly count the prescaled signal. Signal acquisition in the RF band is straightforward: the instrument simply monitors the RF detector. When a signal is detected, the RF gain is adjusted to set the detected signal threshold approximately 3 dB below the peak amplitude and the signal is counted. After every measurement, the RF gain is re-adjusted to ensure rapid tracking of a moving signal. See Figure 7-6, RF Converter Lock Process.

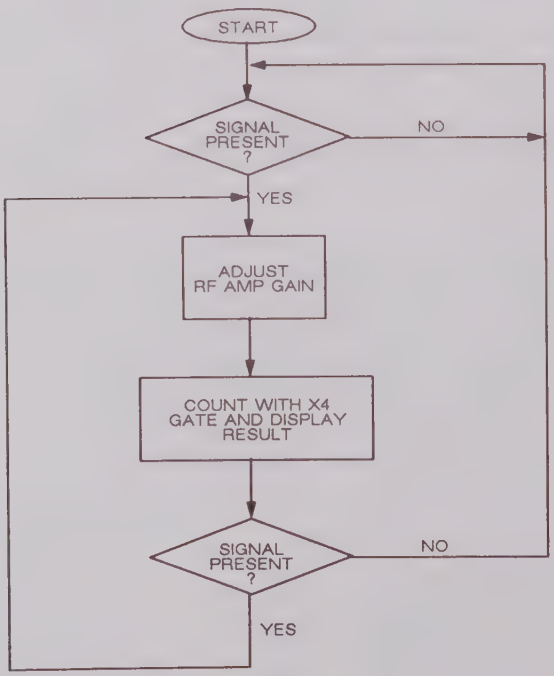



Figure 7-7. RF Converter Lock Process

# Section 8 Functional Description and Illustrated Parts Breakdown

## INTRODUCTION

This section contains a functional description, a parts list, an illustration of componant location, and a schematic diagram for each printed circuit board used in this counter.

The parts list is broken down by types of components, listed in alphanumeric sequence. The components that have a different reference designator (REF DES), but have the same EIP part number, are described for the first such component listed. Subsequent descriptions of that component will refer to the first entry. The total number of like components used on the same assembly will be listed with the first entry in the column identified as UNITS PER ASSY.

The last two columns of the parts list will supply the name of the manufacturer and its Federal Supply Code for Manufacturers (FSCM) number. (See Appendix A).

Pages 8-1 through 8-2 contain the top assembly of the counter and other basic information. After page 8-2, the page numbers begin with an 8 and are followed by a dashed number. The number following the 8 reflects the number of the assembly being described on those pages. The dashed number is the page sequence for that assembly description. For example, pages 85-1 through 85-5 all relate to the A5 printed circuit board assembly. For a diagram of assembly locations in the counter, see Figure 5-1 on page 5-4. A functional block diagram of the counter is included in section 7 on page 7-2.

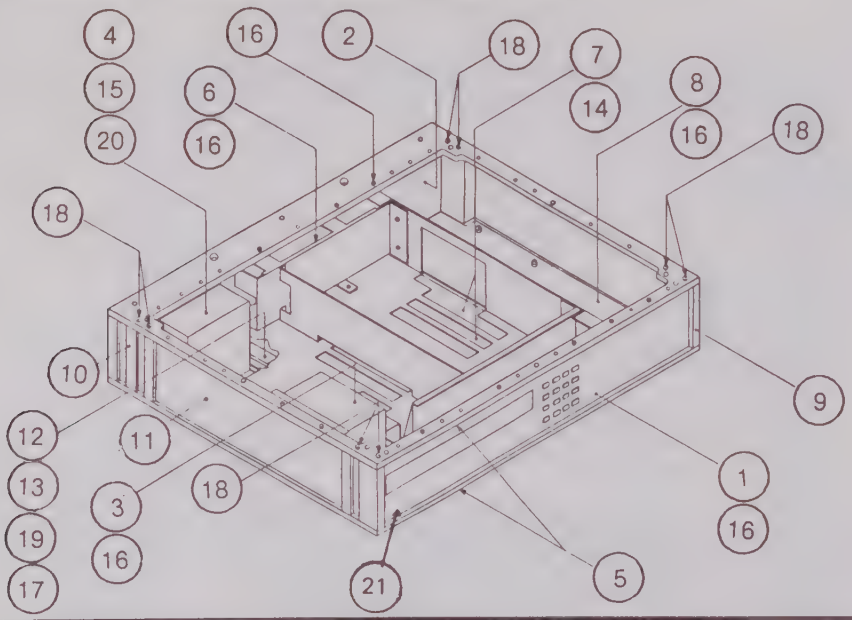
## REFERENCE DESIGNATORS

| | | | |
|---|---|---|---|
| A | Assembly | P | Plug or PCB contacts |
| B | Battery or Fan | Q | Transistor |
| C | Capacitor | R | Resistor |
| CR | Diode | RN | Resistor Network |
| DS | Indicator (display) | S | Switch |
| F | Fuse | T | Transformer |
| J | Jack or Connector | TP | Test Point |
| K | Relay | U | Integrated Circuit |
| L | Inductor | X | Socket or Holder |

## 585/588 ASSEMBLY LISTING 2000028-01

| REF DES. | DESCRIPTION | EIP NO. | UNITS PER ASSY | TYP MFG NO. | TYP FSCM NO. |
|---|---|---|---|---|---|
| A1 | Counter Interconnect | 2020221-01 | 1 | EIP | 34257 |
| A2 | Power Supply | 2020222-01 | 1 | EIP | 34257 |
| A3 | Microprocessor | 2020215-01 | 1 | EIP | 34257 |
| A5 | GPIB/Band 2 Discriminator | 2020218-01 | 1 | EIP | 34257 |
| A6 | Count Chain | 2020219-01 | 1 | EIP | 34257 |
| A7 | Gate Generator | 2020217-01 | 1 | EIP | 34257 |
| A8 | Converter Control | 2020200-03 | 1 | EIP | 34257 |
| A9 | RF (Band 1) Converter | 2020224-01 | 1 | EIP | 34257 |
| A10 | Microwave (Band 2) Converter | 2020296-01 | 1 | EIP | 34257 |
| A11 | Millimeter Wave (Band 3) Converter | 2020238-01 | 1 | EIP | 34257 |
| A12A1 | Front Panel Display/Keyboard | 2020140-02 | 1 | EIP | 34257 |
| A12A2 | Front Panel Logic | 2020191-01 | 1 | EIP | 34257 |
| | Chassis Assy, 585 | 2010354-01 | 1 | | |
| | Chassis Assy, 588 | 2010534-02 | 1 | | |
| | Power Switch | 2010187-02 | 1 | | |
| W3 | Cable Assy, Det Video 1 | 2040288-01 | 1 | | |
| W4 | Cable Assy, Det Video 2 | 2040289-01 | 1 | | |
| W5 | Cable Assy, VCO, Converter Control | 2040263-01 | 1 | | |
| W7 | Cable Assy, VCO, Count Chain | 2040261-01 | 1 | | |
| W8 | Cable Assy, Band 2 IF | 2040260-01 | 1 | | |
| W10 | Harness Assy, 10 MHz | 2040296-01 | 1 | | |
| W11 | Cable Assy, VCO Tuning Voltage | 2040262-01 | 1 | | |
| A12W3 | F/R Cable Assy | 2040169-01 | 1 | | |

FIGURE 8-1. CHASSIS ASSEMBLY, 585/588




| ITEM NO. | DESCRIPTION | EIP NO. | UNITS /ASSY |
|---|---|---|---|
| 1 | Panel, Assy, Front, 585 | 2010284-03 | 1 |
| or | Panel, Assy, Front, 588 | 2010284-04 | 1 |
| 2 | Panel, Assy, Rear, 585/588 | 2010285-01 | 1 |
| 3 | Xfmr Assy, Pwr, 58X | 2010359-01 | 1 |
| 4 | Fan Assy | 2010136-02 | 1 |
| 5 | Frame Assy, RF, 14 in., 58X | 2010313-01 | 2 |
| 6 | Card Cage Assy, 58X | 2010353-01 | 1 |
| 7 | PCB Assy, Counter Interconnect, 58X, A1 | 2020221-01 | 1 |
| 8 | Panel, Microwave Support, 58X | 5210393-00 | 1 |
| 9 | Post, Corner, Front, Black, 2.70 | 5210430-02 | 2 |
| 10 | Post, Corner, Rear, Black, 2.70 | 5210431-02 | 2 |
| 11 | Panel, Side, Vinyl, Blue, 2.81 x 10 in | 5210437-02 | 2 |
| 12 | Spacer | 5210202-00 | 1 |
| 13 | Screw, PNH, X-rec,4-40 x 1/4 unc | 5120004-04 | 2 |
| 14 | Screw, PNH, X-rec,Sems, Intl, 4-40 x 5/16 | 5171004-05 | 15 |
| 15 | Screw, PNH, X-rec,6-32 x 1/4 unc | 5120006-04 | 4 |
| 16 | Screw, PNH, X-rec,Slflkg,6-32 x 3/8 unc | 5124006-06 | 31 |
| 17 | Screw, PNH, X-rec,Sems, Intl, 6-32 x 7/16 | 5171006-07 | 4 |
| 18 | Screw, PNH, X-rec,Slflkg,8-32 x 1/2 unc | 5124008-08 | 16 |
| 19 | Washer, Lk, Intl-T, Cres #4 | 5163004-00 | 1 |
| 20 | Washer, Lk, Intl-T, Cres #6 | 5163006-00 | 4 |
| 21 | Power Switch | 2010187-02 | 1 |

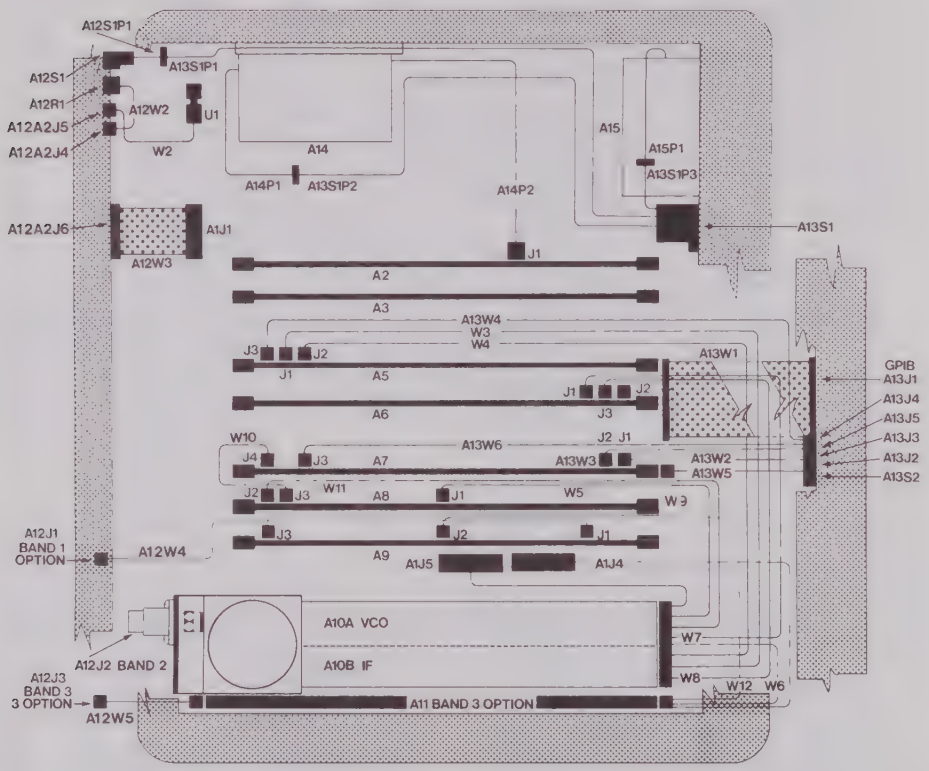



Figure 8-2. 585/588 Cable Guide

# 585/588 CABLE GUIDE

| FROM | CONNECTOR | DESIG. | CONNECTOR | TO | DESCRIPTION |
|---|---|---|---|---|---|
| A12S1P1 | A13S1P1 | A13S1 | A13S1 | REAR PANEL | VOLTAGE SELECT |
| A14P1 | A13S1P2 | A13S1 | A13S1 | REAR PANEL | VOLTAGE SELECT |
| A15P1 | A13S1P3 | A13S1 | A13S1 | REAR PANEL | VOLTAGE SELECT |
| U1 | W2P1 | A16W1 | W2P2 | A12AJ5 | DISPLAY HARNESS |
| A5J1 | W3P1 | W3 | W3P2 | A10J1 | DETECTED VIDEO 1 |
| A5J2 | W4P1 | W4 | W4P2 | A10J2 | DETECTED VIDEO 2 |
| A8J1 | W5P1 | W5 | W5P2 | A10J6 | VCO OUT CONVERTER CONTROL |
| A10J7 | W6P1 | W6 | W6P2 | A11J3 | OPTION: VCO OUT, BAND 3 |
| A6J1 | W7P1 | W7 | W7P2 | A10J5 | VCO OUT, COUNT CHAIN |
| A6J3 | W8P1 | W8 | W8P2 | A10J3 | BAND 2 IF |
| A6J2 | W9P1 | W9 | W9P2 | A9J3 | OPT.: BAND 1/BAND 3 IF |
| A7J4 | W10P1 | W10 | W10P2 | A8J3 | 10 MHz REFERENCE |
| A8J2 | W11P1 | W11 | W11P2 | A10J4 | VCO TUNING VOLTAGE |
| A9J2 | W12P1 | W12 | W12P2 | A11J2 | OPTION: BAND 3 IF |
| | W13P1 | W13 | W13P2 | | |
| A13S1P1 | A12S1P1 | A12S1 | A12S1S1 | FRONT PANEL | POWER SWITCH |
| A12A2J4 | A12W2P1 | A12W2 | A12W2R1 | FRONT PANEL | SAMPLE RATE CONTROL |
| A9J1 | A12W4P1 | A12W4 | A12W4J1 | FRONT PANEL | OPTION: BAND 1 INPUT |
| A11J1 | A12W5P1 | A12W5 | A12W5J3 | FRONT PANEL | OPTION: BAND 3 INPUT |
| A1J2 | A13W1P1 | A13W1 | A13W1J1 | REAR PANEL | GPIB INTERFACE |
| A7J1 | A13W2P1 | A13W2 | A13W2J2 | REAR PANEL | GATE OUTPUT |
| A7J2 | A13W3P1 | A13W3 | A13W3J3 | REAR PANEL | SIGNAL THRESHOLD OUTPUT |
| A5J3 | A13W4P1 | A13W4 | A13W4J4 | REAR PANEL | INHIBIT INPUT |
| A1J3 | A13W5P1 | A13W5 | A13W5S2 | REAR PANEL | 10 MHz INT/EXT SWITCH |
| A7J3 | A13W6P1 | A13W6 | A13W6J5 | REAR PANEL | 10 MHz IN/OUT |
| A9J1 | A13W7P1 | A13W7 | A13W7J6 | REAR PANEL | OPTION: BAND 1 IN, REAR IN |
| A11J1 | A13W8P1 | A13W8 | A13W8J8 | REAR PANEL | OPTION: BAND 3 IN, REAR IN |
| A1J5 | A10P1 | A10 | | | CONVERTER POWER HARNESS |
| A1J4 | A11P1 | A11 | | | BAND 3 HARNESS |
| A2J1 | A14P2 | A14 | | | TRANSFORMER |

## A1 COUNTER INTERCONNECT 2020221-01

| REF DES | DESCRIPTION | EIP NO. | UNITS PER ASSY | TYP MFR NO. | TYP FSCM NO. |
|---|---|---|---|---|---|
| J1 | Conn: 26 Pin PC Header W/E | 2620078-00 | 2 | 3429-2302 | 34257 |
| J2 | J1 | | | | |
| J3 | Conn: 3 Pin PC Rec Lck 156 | 2620201-00 | 1 | 09-65-1031 | 27264 |
| J4 | Conn: 10 Pin PC Rec Lck 156 | 2620092-00 | 1 | 09-65-1101 | 27264 |
| J5 | Conn: 12 Pin PC Rec Lck 156 | 2620143-00 | 1 | 09-65-1121 | 27264 |
| XA2 | Conn: PC Edge 11 Pin | 2620183-00 | 1 | 5193-442-1 | 02660 |
| XA3 | Conn: PC Edge 30 Pin | 2620184-00 | 7 | 5193-442-2 | 02660 |
| XA4 | XA3 | | | | |
| XA5 | XA3 | | | | |
| XA6 | XA3 | | | | |
| XA7 | XA3 | | | | |
| XA8 | XA3 | | | | |
| XA9 | XA3 | | | | |
| | Keying Plug | 5000155 00 | 7 | 530286 2 | 00779 |

## A2 POWER SUPPLY (2020222-01)

The power supply furnishes all basic operating voltages required by the counter. The supply consists of two main circuits:

1. AC line conditioning circuits, consisting of the input power transformer, the input line filter, the voltage select switch, the fuse, and the front panel POWER ON/OFF switch.
2. PC Board A2, containing rectifiers, filter capacitors, and regulator circuitry.

The basic voltages supplied are:

+18 V Unregulated
+12 V
+9 V Unregulated
+5 V
-5.2 V
-12 V

The input ac voltages are full wave rectified and filtered to produce the unregulated dc voltages of +9 V, -9 V, +18 V, and -18 V.

+18 V The unregulated 18 volts is used directly as one supply voltage for the microwave converter.

+12 V The +18 volts is regulated to +12 volts by an LM317 three-terminal series regulator employing thermal current protection.

+9 V The unregulated 9 volts is used to drive the front panel, and is regulated to +5 V at the front panel.

+5 V The +5 volts is regulated by a single three-terminal regulator from the +9 volts unregulated supply. This regulator contains internal current and thermal sensing circuitry.

-5.2 V The -5.2 volts is also regulated by a single three-terminal regulator. The -9 volt unregulated supply is used for this regulator. This regulator also contains internal thermal and current shutdown circuitry.

-12 V -18 volts is regulated to -12 volts by the action of an LM337 three-terminal series regulator employing thermal current protection.

## A2 POWER SUPPLY 2020222-01

| REF DES. | DESCRIPTION | EIP NO. | UNITS PER ASSY | TYP MFG NO. | TYP FSCM NO. |
|---|---|---|---|---|---|
| C1 | Elect 32,000µF 15 | 2200019-00 | 1 | 110RB323U015 | 80031 |
| C2 | Elect 27,000µF 15 | 2200027-00 | 1 | 186BD273U015 BMAI | 80031 |
| C3 | Tant, 10µF, 25V | 2300029-00 | 4 | TAPA10M25 | 14433 |
| C4 | Elec, 14,000µF, 25V | 2200017-00 | 1 | 3110HB143u025 | 80031 |
| C5 | Elec, 9,500µF, 25V | 2200016-00 | 1 | 3110BA52u025AP | 80031 |
| C6 | C3 | | | | |
| C7 | Tant, 1.0µF, 35V | 2300008-00 | 4 | TAPA1.0M35 | 14433 |
| C8 | C3 | | | | |
| C9 | C7 | | | | |
| C10 | C3 | | | | |
| C11 | C7 | | | | |
| C12 | C7 | | | | |
| CR1 | Bridge, 50V | 2710029-00 | 1 | MDA 970-1 | 04713 |
| CR2 | Bridge | 2710028-00 | 1 | MDA 990-1 | 04713 |
| J1 | Conn, 6 Pin, Fr Lock | 2620157-00 | 1 | 640445-6 | 17105 |
| J2 | Conn, 3 Pin, Fr Lock | 2620154-00 | 1 | 640445-3 | 17105 |
| U1 | Reg, 5V-5A, 4%, 50W | 3057805-01 | 1 | UA78H05A | 07263 |
| U2 | +12V Reg, 3-Terminal | 3040317-00 | 1 | LM317T | 27014 |
| U3 | -12V Reg, 3-Terminal | 3040337-00 | 1 | LM337T | 27014 |
| U4 | -5.2V Reg | 3040345-00 | 1 | LM345K | 27014 |
| TP1 thru TP4 | Conn, Pin-TP, Swage .040D- 15( L | 2620193-00 | 4 | | |
| R1 | MF, 475, 1%,1/10W | 4054750-00 | 1 | RN55C4750F | 24546 |
| R2 | MF, 3.01K, 1%, 1/10W | 4053011-00 | 1 | RN55C3011F | 91637 |
| R3 | Pot-CR, 2K, 1/2W | 4250016-00 | 2 | 72XR2K | 80740 |
| R4 | CC, 5.1, 5%,1W | 4030519-00 | 2 | RC32GF5R1J | 01121 |
| R5 | R4 | | | | |
| R6 | R3 | | | | |
| R7 | MF, 8.66K, 1%, 1/8W | 4068661-00 | 1 | RN55D866IF | 24546 |
| R8 | MF, 1.21K, 1%, 1/10W | 4051211-00 | 1 | RN55C1211F | 24546 |
| R9 | Met Ox, 200, 1/4W, 2% | 4130201-00 | 1 | RL07S201G | 24546 |
| R10 | CC, 5.6, 1/4W, 5% | 4010569-00 | 1 | RC07GF5R6J | 01121 |
| R11 | Met Ox, 13, 1/4W, 2% | 4130130-00 | 1 | RL073130G | 24546 |
| R12 | CC, 4.7, 1/4W, 5% | 4010479-00 | 1 | RC07GF4R7J | 01121 |

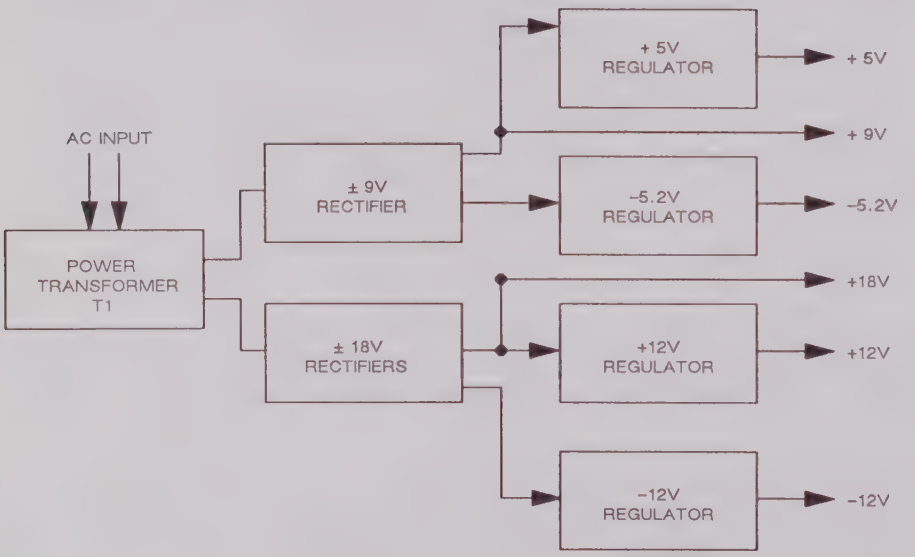



Figure 82-1. Functional Block Diagram, Power Supply

## A3 MICROPROCESSOR (2020215-01)

The Microprocessor board contains the microprocessor, the control logic, and the firmware for controlling the operation of the counter. The board can be divided into five functional blocks.

- Microprocessor
- Power-up Reset Circuit
- Address Decoder
- RAM and Program Memory
- Control Logic Buffers.

### MICROPROCESSOR

The counter uses a Motorola 6809 microprocessor. The clock generation circuitry for the digital system is contained within the 6809. The only external components required for clock generation are two 24-pF capacitors and an AT-cut 4-MHz crystal.

The NMI, FIRQ, and DMA functions of the 6809 are not used. Their corresponding control lines are always disabled. The processor state indicators (BS, BA) are also not used by the counter. The HALT and the MRDY controls are connected to the Interconnect board through the edge connector.

### POWER-UP RESET CIRCUIT

The Power-up Reset circuit provides a 100-ms reset signal to the entire digital system after the counter is turned on. The reset remains true as long as the +5-volt power supply stays below +4 volts.

When the counter is turned on, the voltage across C5 is 0 volts. The output of the comparator U1 is at logic low. The capacitor C5 slowly charges up through R2. The output of the comparator remains low as long as the voltage across C5 is lower than the voltage on pin 3 of the comparator. When the voltage across C5 becomes higher than that on pin 3, the output of the comparator becomes true, removing the reset signal. R3 is provided for hysteresis purposes. When power is removed, C5 will discharge quickly through CR1.

## ADDRESS DECODER

The address decoding is performed by a 4-to-16 line decoder. The 64K-byte address space is divided into sixteen 4K-byte blocks, one of which is always enabled.

The enable signals for the memory blocks become true no later than 51 ns after Q. They stay true until a maximum of 40 ns after E has become false. The 4-to-16-line decoder has open collector outputs. This enables the addressed memory block to be enlarged by wire-ORing two or more outputs together.

The memory map for the counter is as follows:

| | |
|---|---|
| Volatile RAM Memory | 0000 - 07FF |
| Non-Volatile RAM Memory | 0800 - 0FFF |
| I/O | 1000 - 2FFF |
| Signature Analysis | 3000 - 3FFF |
| Program Memory | 4000 - FFEF |
| Reserved (6809) | FFF0 - FFF1 |
| SW13 | FFF2 - FFF3 |
| SW12 | FFF4 - FFF5 |
| FIRQ | FFF6 - FFF7 |
| IRQ | FFF8 - FFF9 |
| SWI | FFFA - FFFB |
| NMI | FFFC - FFFD |
| RESET | FFFE - FFFF |

## RAM AND PROGRAM MEMORY

### RAM

A 2K-byte-wide volatile RAM is provided for the normal operation of the counter. To prevent data from being erroneously written into the RAM, the chip enable signal is active only when the E clock and the RAM memory block enable signal from the address decoder are both active and when the A11 address line is at logic 1.

### PROM

A block of 48K bytes of memory are assigned for system program. The Microprocessor board contains three 28-pin sockets for PROMs. Each of the sockets are wired to accept a 16K-byte PROM.

The digital system of the counter contains three buses: the data bus, the address bus, and the control bus.

## DATA BUS

The data bus originates from the microprocessor. For signature analysis, the data bus can be disconnected from the rest of the system at the microprocessor by removing jumper header E1 and installing it in E2. The data bus on the microprocessor board is buffered from the rest of the digital system. The data bus buffer is enabled only when the address space assigned to I/O is addressed. The direction of the data bus buffer is determined by the state of the R/W control line.

## ADDRESS BUS

The address bus also originates from the microprocessor. The address bus buffer is always enabled.

## CONTROL BUS

The control bus contains eight control lines. Five of the control lines originate from the Microprocessor board. The other three control lines originate from the rest of the digital system.

R/W, E, and Q originate from the microprocessor. Reset is supplied by the power-up reset circuit. The I/O SEL control line is true when A15 and A14 are at logic 0 and either A13 or A12 or both are at logic 1 levels. The IRQ control line is the wired-OR of all the interrupt request lines. MRDY is the wired-OR of all the memory ready control lines. The MRDY and HALT control lines are provided for future expansion.

## A3 MICROPROCESSOR 2020215-01

| REF DES | DESCRIPTION | EIP NO. | UNITS PER ASSY | TYP MFR NO. | TYP FSCM NO. |
|---|---|---|---|---|---|
| C1 | Mica, 24pF, 5%, 500V | 2260018-00 | 2 | CD10ED240J03 | 14655 |
| C2 | C1 | | | | |
| C3 | Disc, 0.01μF, 20%, 100V | 2150003-00 | 14 | TG - S10 | 56289 |
| C4 | C3 | | | | |
| C5 | Tant, 3.9μF, 10%, 15V | 2300027-00 | 1 | 196D395X9015HA1 | 56289 |
| C6 | C3 | | | | |
| C7 | C3 | | | | |
| C8 | C3 | | | | |
| C9 | Tant, 33μF, 10V | 2300015-00 | 2 | TAPA33M10 | 14433 |
| C10 | C3 | | | | |
| C11 | C3 | | | | |
| C12 | C3 | | | | |
| C13 | C3 | | | | |
| C14 | C3 | | | | |
| C15 | C3 | | | | |
| C16 | C3 | | | | |
| C17 | C3 | | | | |
| C18 | C3 | | | | |
| C19 | C9 | | | | |
| CR1 | H/C | 2710004-00 | 1 | 5082-2835 | 07263 |
| CR2 | Zener, 3.9V | 2705228-00 | 1 | IN5228 | 04713 |
| R1 | Met Ox, IM, 5%, 1/4W | 4010105-00 | 1 | RC07GF105J | 81349 |
| R2 | Met Ox, 22K, 5%, 1/4W | 4010223-00 | 1 | RC07GF223J | 81349 |
| R3 | Met Ox, 300K, 5%, 1/4W | 4010304-00 | 1 | RC07GF304J | 81349 |
| R4 | Not used | | | | |
| R5 | Met Ox, 240, 5%, 1/4W | 4010241-00 | 1 | RC07GF241J | 81349 |
| R6 | Met Ox, 4.7K, 5%, 1/4W | 4010472-00 | 4 | RC07GF472J | 81349 |
| R7 | R6 | | | | |
| R8 | R6 | | | | |
| R9 | R6 | | | | |
| RN1 | Res. Network, 9 x 10k, 2%, 2W | 4170003-00 | 3 | 782-1-R10K | 80740 |
| RN2 | RN1 | | | | |
| RN3 | RN1 | | | | |
| RN4 | Res. Network, 9 x 4.7k, 2%,1.25W | 4170014-00 | 1 | 4310R-101-472 | 32997 |
| TP1-10 | Pin, T.P. Swage | 2620032-00 | 10 | 460-2970-02-03 | 71279 |
| U1 | Int: Volt Comparator | 3050311-00 | 1 | MLM311P1 | 27014 |
| U2 | Microprocessor | 3056809-00 | 1 | MC6809 | 04713 |
| U3 | Dvr Hex Bus/Buffer | 3084365-00 | 1 | SN74LS365N | 01295 |
| U4 | Not Used | | | | |
| U5 | 3-Inp NOR Gate | 3087427-00 | 1 | DM74LS27 | 27014 |
| U6 | Dvr Line/Oct Buf Invg | 3084244-00 | 2 | SN74LS244N | 01295 |
| U7 | Not Used | | | | |

## A3 MICROPROCESSOR (Continued) 2020215-01

| REF DES | DESCRIPTION | EIP NO. | UNITS PER ASSY | TYP MFR NO. | TYP FSCM NO. |
|---|---|---|---|---|---|
| U8 | Xcvr Octal Bus | 3084245-00 | 1 | SN74LS245N | 01295 |
| U9 | 2K x 8 CMOS RAM | 3056116-00 | 1 | HM6116LP-4 | 62786 |
| U10 | 2K x 8E PROM | 6420000-00 | 1 | X2816A | 60395 |
| U11 | PROM Set: 16K x 8 | 2060006-01 | 1 | 27128 | |
| U12 | U11 | | | | |
| U13 | U11 | | | | |
| U14 | 3-Inp NAND Gate | 3087410-00 | 1 | DM74LS10 | 27014 |
| U15 | U6 | | | | |
| U16 | 4-16 Decoder | 3074159-00 | 1 | SN74159N | 01295 |
| U17 | Hex Inverter | 3087404-00 | 1 | DM74LS04 | 27014 |
| E1 | Prog. Header, 16 Pin DIP | 5000205-00 | 1 | 16-675-191T | 51167 |
| Y1 | Xtal, 4.00 MHz | 2030015-00 | 1 | MP-1 | ATRON |

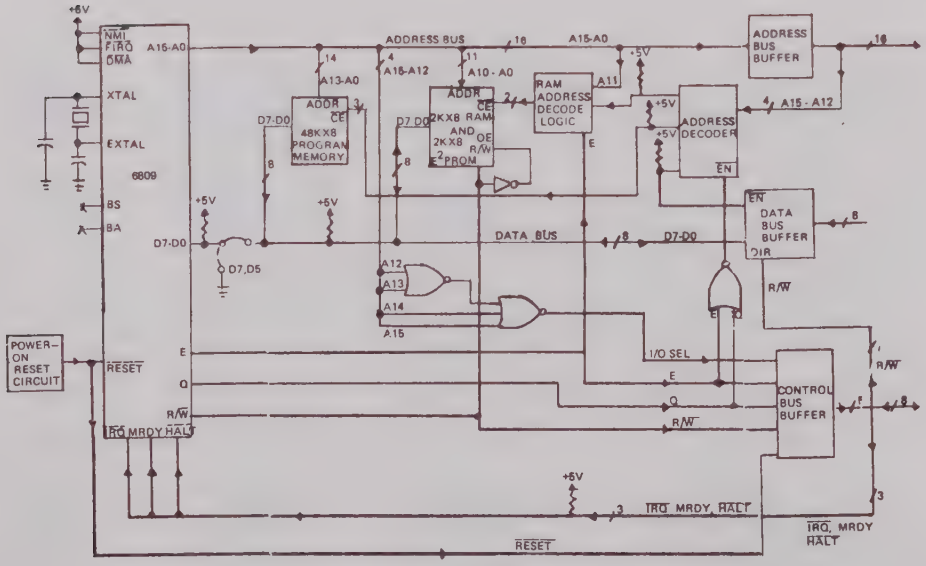



Figure 83-1. Functional Block Diagram, Microprocessor

# A5 GENERAL PURPOSE INTERFACE BUS (GPIB)/ MICROWAVE (BAND 2) POWER DISCRIMINATOR (2020218-01)

The GPIB board performs two major functions:

- GPIB interface
- Band 2 amplitude determination, in conjunction with the Detector/Video Amplifier in the Band 2 converter module.

## GPIB INTERFACE

The GPIB interface makes the 58X counter fully compatible with IEEE 488-1978. The functions implemented are:

- Basic talker with talk only
- Basic listener
- Remote/local with local lockout
- Device clear
- Device trigger
- Service request

The address decoder consists of U5 and U6. They enable the TI9914 GPIB interface adapter (GPIA) at hexadecimal addresses 1C00 through 1C07 and the 8-bit DAC at hexadecimal address 2A00.

Transceivers U2 and U3 provide the required bus buffering and termination for the GPIB. They are driven directly from the GPIA.

U1 is the TI9914 GPIB interface adapter. It performs all the bus functions and protocols according to commands from the microprocessor. All data and messages between the microprocessor and the GPIB are transferred through this IC.

## BAND 2 AMPLITUDE DETERMINATION

The amplitude determination circuit converts the analog signals at J1 and J2 into digital information for the microprocessor. The signals at J1 are derived from video amplifiers driven by a square law detector. The signal amplitude at J2 is 40 times the amplitude at J1.

The A/D converters (U14, U15, U16, and U17) perform a fast conversion of the signal at J1 and J2 into digital signals for the microprocessor. Dynamic range is 30 dB and resolution is 1.25 dB.

The A/D converters, consisting of eight comparators arranged in two sets of four comparators each, compare video inputs at J1 and J2 to reference levels. The comparator reference levels are set by resistive voltage dividers at 5 dB apart and are driven by the eight-bit DAC (U7).

The eight-bit DAC is driven directly from the microprocessor and provides the reference signal for the A/D converters. The DAC output varies from 2.5 to 8 volts (6 dB) and is stepped in 1.25-dB increments.

The latches consist of eight cross-coupled NAND gates (U12 and U13) that hold the comparator outputs for the microprocessor through the PIA (U8) and NAND gate U9A.

The rear panel INHIBIT INPUT connector is connected to J3. The inhibit signal passes through ECL-to-TTL converter U11 to U9C and U10. The output of U10, a TTL-to-ECL converter, goes to the Gate Generator board and disables the gate signal while inhibit is true. The inhibit signal from U10 can be disabled by the microprocessor through U9D.

## A5 GPIB/BAND 2 POWER DISCRIMINATOR 2020218-01

| REF DES | DESCRIPTION | EIP NO. | UNITS PER ASSY | TYP MFR NO. | TYP FSCM NO. |
|---|---|---|---|---|---|
| C1 | Disc .01μF 100V | 2150003-00 | 13 | TG-S10 | 51406 |
| C2 | C1 | | | | |
| C3 | Cer 33pF 100V | 2150069-00 | 1 | 5018E0100RD330K | 29938 |
| C4 | C1 | | | | |
| C5 | C1 | | | | |
| C6 | C1 | | | | |
| C7 | C1 | | | | |
| C8 | C1 | | | | |
| C9 | C1 | | | | |
| C10 | C1 | | | | |
| C11 | C1 | | | | |
| C12 | C1 | | | | |
| C13 | Tant. 33μF 10V | 2300015-00 | 2 | TAPS33M10 | 14433 |
| C14 | Tant. 10μF 25V | 2300029-00 | 2 | DF106M25S | 76718 |
| C15 | C14 | | | | |
| C16 | C13 | | | | |
| C17 | C1 | | | | |
| C18 | C1 | | | | |
| R1 | Met Ox 1K 2% 1/4W | 4130102-00 | 1 | C4/2%/1K | 24546 |
| R2 | Met Ox 270 2% 1/4W | 4130271-00 | 3 | C4/2%/270 | 24546 |
| R3 | Met Ox 560 2% 1/4W | 4130561-00 | 3 | C4/2%/560 | 24546 |
| R4 | Met Ox 100 2% 1/4W | 4130101-00 | 1 | C4/2%/100 | 24546 |
| R5 | R2 | | | | |
| R6 | R2 | | | | |
| R7 | Met Ox 160 2% 1/4W | 4130161-00 | 3 | C4/2%/160 | 24546 |
| R8 | R7 | | | | |
| R9 | R3 | | | | |
| R10 | R7 | | | | |
| R11 | Met Ox 68 2% 1/4W | 4130680-00 | 1 | C4/2%/68 | 24546 |
| R12 | Met Ox 33 2% 1/4W | 4130330-00 | 1 | C4/2%/33 | 24546 |
| R13 | Met Ox 20 2% 1/4W | 4130200-00 | 1 | C4/2%/20 | 24546 |
| R14 | R3 | | | | |
| R15 | Met Ox 51 2% 1/4W | 4130510-00 | 2 | C4/2%/51 | 24546 |
| R16 | Met Ox 180 2% 1/4W | 4130181-00 | 1 | C4/2%/180 | 24546 |
| R17 | Met Ox 62 2% 1/4W | 4130620-00 | 1 | C4/2%/62 | 24546 |
| R18 | Met Ox 22 2% 1/4W | 4130220-00 | 1 | C4/2%/22 | 24546 |
| R19 | Met Ox 10 2% 1/4W | 4130100-00 | 1 | C4/2%/10 | 24546 |
| R20 | R15 | | | | |
| U1 | GPIB Controller | 3059914-00 | 1 | TMS9914 | 01295 |
| U2 | Bus Driver | 3055161-00 | 1 | SN 75161 | 01295 |
| U3 | Bus Driver | 3055160-00 | 1 | SN 75160 | 01295 |
| U4 | Op. Amp Buff | 3040308-00 | 1 | LM308AN | 27014 |
| U5 | Quad 2-Inp OR Gate | 3087432-00 | 1 | DM74LS 32 | 27014 |
| U6 | Quad 2-Inp NAND Gate | 3087400-00 | 2 | DM74LS 00 | 27014 |
| U7 | DAC 8 Bit 1/2 LSB | 3057524-00 | 1 | AD7524JN | 01884 |

## A5 GPIB/BAND 2 POWER DISCRIMINATOR (Continued) 2020218-01

| REF DES | DESCRIPTION | EIP NO. | UNITS PER ASSY | TYP MFR NO. | TYP FSCM NO. |
|---|---|---|---|---|---|
| U8 | PIA TO MC6800 | 3086820-00 | 1 | MC6820P/6821P | 04713 |
| U9 | U6 | | | | |
| U10 | Quad Mecl | 3110124-00 | 1 | MC10124L | 04713 |
| U11 | Dig Quad. Translator | 3110125-00 | 1 | MC10125L | 04713 |
| U12 | Quad S-R Latch | 3084279-00 | 2 | DM74S279 | 27014 |
| U13 | U12 | | | | |
| U14 | Dual Comparator | 3050521-00 | 4 | NE521N | 18324 |
| U15 | U14 | | | | |
| U16 | U14 | | | | |
| U17 | U14 | | | | |
| CR1 | Hot Carrier | 2710004-00 | 2 | 5082-2835 | 28480 |
| CR2 | CR1 | | | | |
| Q1 | NPN GP | 4704124-00 | 1 | 2N4124 | 04713 |
| J1 | Conn, Mini PC Jack | 2610038-00 | 3 | 51-451-0000 | 98291 |
| J2 | J1 | | | | |
| J3 | J1 | | | | |

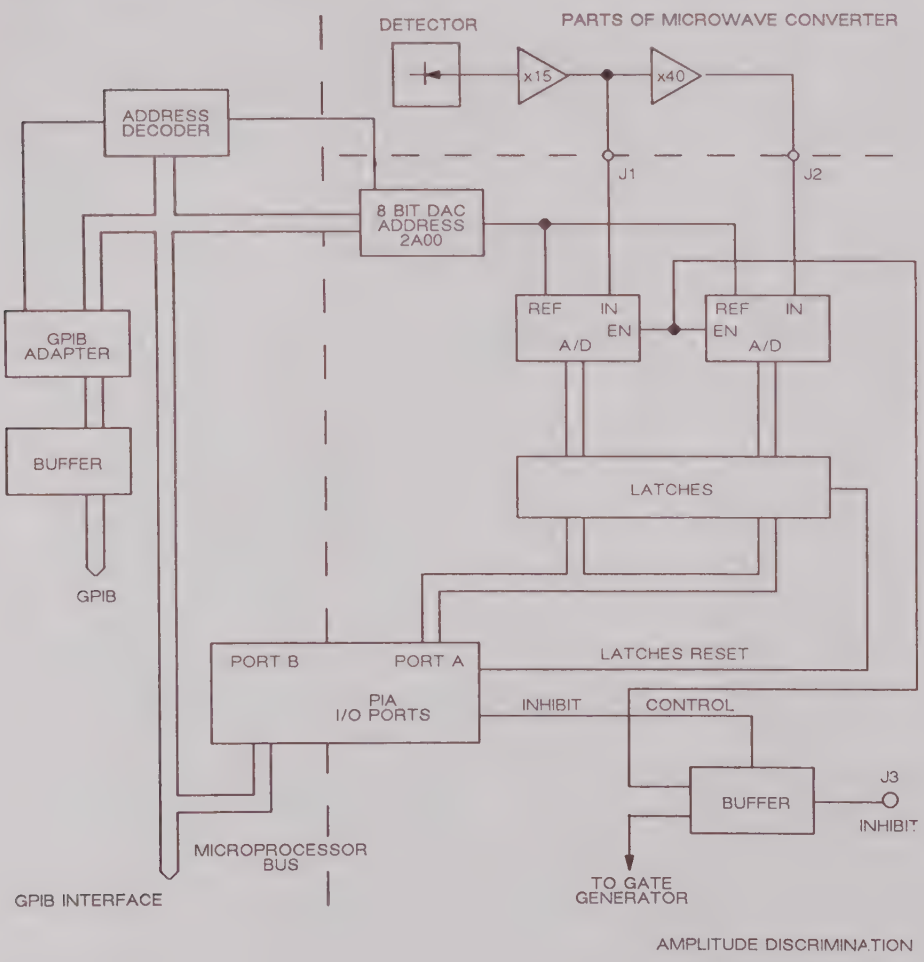



Figure 85-1. Functional Block Diagram, GPIB/Band 2 Power Discriminator

## A6 COUNT CHAIN (2020219-01)

The primary function of this board is to count the number of zero crossings of an input signal in a given period of time, called the gate. The input signal may be the IF of the measured signal in the frequency mode, or the signal output by the VCO in the pulse parameter measurement and self test modes.

A second function is to detect the Band 2 IF, and a third function is to provide the real-time clock for the counter.

The Count Chain assembly consists of following functional blocks:

- IF Delay Circuit
- Divide-by-Four Prescaler
- Band 2 IF Detector
- IF Pulse-Shaping Network
- Gate Width Adjustment
- IF Frequency Measurement
- Real-Time Clock

In addition, there are two switches:

- IF/Prescaler Selector — selects between the IF signal and the Divide-by-Four Prescaler.
- Detected Signal Selector — selects between the Band 2 and the Band 1 or 3 detected signal.

Control and timing of the Count Chain board signals are performed by the microprocessor through a peripheral interface adapter (PIA).

## SIGNAL PATH

The IF signal is distributed between the IF Delay circuit and the Band 2 IF Detector. The IF Delay Circuit delays the signal in order to adjust its timing to that of the gate signal. The Detected Signal Selector transfers the appropriate detected IF band to the Gate Generator board. The detected IF is processed by the Gate Generator board and brought back to the Gate Width Adjustment block. There it is compensated for gate error and for minor changes in the gate width caused by passing the signal through the digital gates and the lines on the Interconnect board.

When the counter is in the frequency measurement mode, the IF signal coming from the delay line passes through the IF/Prescaler Selector to the Pulse-shaping Network. The waveform at this input consists of very short pulses (0.5 ns) at the point of zero crossing.

The Pulse-shaping Network output is connected to the gate input of the BCD counter (the IF Frequency Measurement block).

When the counter is in the pulse parameter measurement mode, the gate signal input to the IF/Frequency Measurement block is the width or the period of the signal. The IF/Prescaler Selector is connected to the Divide-by-Four Prescaler. Therefore the counter measures a known frequency of the VCO output divided by four, that is, 100 to 125 MHz. The counter then computes the parameters according to the number of cycles it counts.

When the counter is in the test mode, both switches cause the detected signal channel to have a constant threshold and the IF signal is fed from the Divide-by-Four Prescaler at a constant frequency of 100 MHz.

## IF DELAY CIRCUIT

The Band 2 IF signal (through connector J3) or the Band 1 or 3 signal (through connector J2) is passed to the input of U2C pins 12 or 13 respectively. U2 is an ECL line receiver used here as a differential amplifier. The microprocessor ensures that the two signals do not exist simultaneously. The output is connected to a 45-ns delay line (approximately 30 feet of coax cable) terminated with 50 ohms of resistance (R7 and R9 in parallel).

## DIVIDE-BY-FOUR PRESCALER

The input to the Divide-by-Four, U1 pin 3, (through J1 connector) is the output of the VCO, a 400 to 505 MHz CW signal that exits only in the self-test and pulse parameter modes of operation. The prescaler U1 divides the frequency by four, and sends its output to U3 pin 10. Since U1 oscillator without any input, it is disabled by Q1 and R3. This resistor is floating when the counter is in either the self-test or the pulse parameter modes and Q1 is off, permitting U1 to divide.

When the counter is in the frequency measurement mode, R3 is connected to +12 volts via Q1, changing the bias condition of the Divide-by-Four Prescaler and disabling the oscillation. It takes the divider approximately 10 microseconds to pass from an idle to a dividing state. The switching command is sent from the PIA (pin 39) through U5A, an open-collector TTL inverter.

The Band 2 IF signal (connector J3) is distributed to U2C and U2A. The latter (with R90 and C21) forms a peak-positive detector. The output of this detector is a video signal corresponding to the envelope of the IF signal. This video signal goes through a Schmitt trigger circuit (U4), which shapes the analog signal to ECL levels with fast rise and fall times. The circuit uses all three U4 line receivers to provide more than 30 dB gain.

Band 2 IF detector uses R22 as the feed-back resistor, giving the circuit the necessary amount of hysteresis to be immune to noise and spikes. U2B provides a reference voltage of VBB, which precisely tracks the bias voltage of the detector.

## IF PULSE-SHAPING NETWORK

The IF from either the IF Delay Circuit or the Divide-by-Four Prescaler is input to the line receiver/differential amplifier U3 (pins 10 or 9 respectively). The output differentially drives a wide-band high-speed differential amplifier (Q3 and Q4). The differential outputs of this amplifier drive current switch Q5. The resulting current square wave from Q5 drives inductor L2, producing a series of positive pulses when Q5 turns on and negative pulses when it turns off. These pulses are input to a pulse inverter, Q7. Q7 acts as a high-speed zero-crossing amplifier, because it is biased at cut-off by Q9. (Q9 performs as a diode. It is the same type of transistor as Q7, used for precise tracking over temperature). The Q7 amplifier inverts the positive pulses and removes the unwanted negative pulses. The output of the pulse inverter drives the input of the IF Frequency Measurement block (BCD counter).

## IF FREQUENCY MEASUREMENT

The IF Frequency Measurement block consists of three major parts:

1. A divide-by-ten unit with binary coded decimal outputs (U7) and a surrounding bias circuit
2. An asynchronous four-bit decade counter (U11)
3. A six-decade up-counter with eight-decade latches and multiplexed BCD output (U12).

The IF Frequency Measurement block gets its input frequency at U7 pin 14 from the Pulse-shaping Network, its gate at U7 pin 16 from the Gate Width Adjustment block, and, in response to the microprocessor commands, outputs the frequency readings at U12, pins 17, 18, 19, and 20.

The bias point for U7 pin 14 input is established by a tracking bias circuit (U9 and Q6) whose output is equal to the voltage on U7 pin 1, plus a fixed dc voltage offset selected by resistors R62 and R63. This bias determines the threshold voltage of a U7 internal comparator.

The divide-by-ten output of the U7 decade counter is a 40/60 duty cycle ECL level signal. It is converted to TTL by U10, an ECL tc TTL translator, which in turn drives a second decade counter, U11.

The BCD outputs of U7 and U11 are connected to a VLSI counter, IC U12, which derives its clock information at pin 28 (B8) directly from the D output of U11 (Pin 11). The TTL-compatible BCD outputs of U7 are very slow compared to its carry output (pin 9). As a result, these outputs will only settle to a defined state when the gate signal is removed.

When a count cycle is completed, eight decades of BCD data are read by the microprocessor (through the PIA U13) by a time multiplex process. The U12 multiplexer (set to the first digit by the end of the previous reset clock) loads the multiplex latches with the load clock (pin 21), and steps to the remaining seven digits with seven pulses on the scan clock line. A single reset line resets all count stages to zero before the next count cycle begins.

## GATE WIDTH ADJUSTMENT

The Gate Width Adjustment circuitry compensates for minute errors in the gate signal width caused by the digital circuitry. This is especially important in Band 1 and Band 3, where the higher frequency of the IF allows for greater frequency error. The gate signal enters the board on differential lines at the edge connector pins 6 and 36. The signal is input to U8A, a line receiver. Its output drives another line receiver acting as a differential inverting amplifier. The threshold signal for this second line receiver is derived from operational amplifier U15. Its output tracks the reference voltage on U8 pin 11 plus a fixed offset supplied by the voltage divider and digital-to-analog converter (DAC), consisting of U14 and U16. This accommodates slight changes in threshold that produce a change in gate width. The output of this circuit, consisting of U8 and U15, drives the clock enable input of U7 pin 16.

The function of the DAC is to change the bias in such a way that correction of gate error can be done by software control. The error correction factors are stored in non-volatile RAM. This enables automatic calibration of the gate signal.

## REAL-TIME CLOCK

The Real-time Clock, U17, delivers a 100-Hz square wave to the PIA, U13 pin 18. It is used for timing the flashing of the annunciators and for timing the intervals between loss of IF threshold checks.

## IF/PRESCALER SELECTOR

When the IF signal is counted, the PIN diode CR1 is forward biased with 10 mA of current supplied by Q2. At the same time, Q1, through R3, changes the bias conditions at U3 pin 3 so it will not oscillate. At these times, an IF signal reaches U3 pin 9 while no signal is present at pin 10.

When the VCO output is counted, Q1 and Q2 are cut off. Diode CR1 is isolated and attenuates the IF channel by approximately 20 dB. R3 is floating and U1 is enabled to divide the VCO input. Q1 and Q2 are controlled by the microprocessor through U5A.

## DETECTED SIGNAL SELECTOR

This circuit selects either the Band 2 detected IF signal or the Band 1 or 3 detected IF signal and sends it through U6 pins 6 and 7 on differential lines to the Gate Generator board. The Band 2 detected IF signal is connected to U6 pin 4. The Band 1 or 3 detected IF enters the board differentially on the edge connector pins 8 and 38. It is then converted to an unbalanced signal by line receiver U3B, which delivers it to U6 pin 12. U6 is used as a multiplexer and is controlled by the microprocessor through U5B and U5F.

When U6 pin 5 is low and U6 pin 13 is high, the Band 2 detected IF is sent to the Gate Generator board on the edge connector pins 4 and 34. When U6 pin 13 is low and pin 5 is high, the Band 1 or 3 detected IF is sent to the Gate Generator board, and when both U6 pins 5 and 13 are high, the Gate Generator receives a constant IF threshold (for the 100-MHz self test).

## A6 COUNT CHAIN 2020219-01

| REF DES | DESCRIPTION | EIP NO. | UNITS PER ASSY | TYP MFR NO. | TYP FSCM NO. |
|---|---|---|---|---|---|
| C1 | Cer, 0.01µF, 10%, 100V | 2150014-00 | 12 | 5020EM100RD103K | 29938 |
| C2 | C1 | | | | |
| C3 | Cer, 0.001µF, 10%, 100V | 2150015-00 | 24 | 5018EM100RD102K | 29938 |
| C4 | C3 | | | | |
| C5 | C1 | | | | |
| C6 | C3 | | | | |
| C7 | C3 | | | | |
| C8 | C1 | | | | |
| C9 | C1 | | | | |
| C10 | C1 | | | | |
| C11 | C3 | | | | |
| C12 | C3 | | | | |
| C13 | X7R, 0.1µF, 50V | 2150028-00 | 3 | RC50-104KB | 51406 |
| C14 | C3 | | | | |
| C15 | C3 | | | | |
| C16 | Cer, 6.8pF,100V | 2150087-00 | 1 | 5018E0100RD689K | 29938 |
| C17 | C1 | | | | |
| C18 | C3 | | | | |
| C19 | C3 | | | | |
| C20 | C3 | | | | |
| C21 | Cer, 100pF, 100V | 2150056-00 | 1 | 5018EM100RD101K | 29938 |
| C22 | Cer, XCR, .01µF, 10%, 50V | 2100040-00 | 4 | 1206B103K2T | 95275 |
| C23 | C1 | | | | |
| C24 | C1 | | | | |
| C25 | C22 | | | | |
| C26 | C22 | | | | |
| C27 | Chip, 0.001µF, 50V | 2100002-00 | 3 | VJ1210A102MF | 95275 |
| C28 | C22 | | | | |
| C29 | C27 | | | | |
| C30 | Tant, 10µF, 25V | 2300029-00 | 4 | DF106M25S | 76718 |
| C31 | C30 | | | | |
| C32 | C3 | | | | |
| C33 | C1 | | | | |
| C34 | Cer, 33pF, 10%, 100V | 2150069-00 | 3 | 5018E0100RD330K | 29938 |
| C35 | C3 | | | | |
| C36 | C3 | | | | |
| C37 | C13 | | | | |
| C38 | C13 | | | | |
| C39 | C1 | | | | |
| C40 | C3 | | | | |
| C41 | C3 | | | | |
| C42 | C34 | | | | |
| C43 | C3 | | | | |
| C44 | C3 | | | | |
| C45 | C34 | | | | |
| C46 | C3 | | | | |
| C47 | C3 | | | | |

## A6 COUNT CHAIN (Continued) 2020219-01

| REF DES | DESCRIPTION | EIP NO. | UNITS PER ASSY | TYP MFR NO. | TYP FSCM NO. |
|---|---|---|---|---|---|
| C48 | C3 | | | | |
| C49 | C3 | | | | |
| C50 | C1 | | | | |
| C51 | C3 | | | | |
| C52 | Tant, 33μF, 10V | 2300015-00 | 4 | TAPA33M10 | 14433 |
| C53 | C52 | | | | |
| C54 | C30 | | | | |
| C55 | C30 | | | | |
| C56 | C3 | | | | |
| C57 | Not Used | | | | |
| C58 | C52 | | | | |
| C59 | C27 | | | | |
| C60 | C52 | | | | |
| C61 | Cer, 220pF, 10%, 100V | 2150047-00 | 1 | 100-100-XR7-221K | 51642 |
| C62 | Cer, 33pF, 10%, 100V | 2150037-00 | 1 | 100-100-XR7-330K | 51642 |
| CR1 | Pin | 2710024-00 | 1 | MA47123 | 96067 |
| CR2 | Zener, 6.2 V | 2705234-00 | 1 | IN5234 | 04713 |
| CR3 | Zener, 5.1 V | 2705231-00 | 1 | IN5231 | 04713 |
| CR4 | H/C | 2710004-00 | 1 | 5052-2835 | 28480 |
| J1 | Conn, Coax PC Snap-On | 2610038-00 | 6 | 51-451-0000 | 98291 |
| J2 | J1 | | | | |
| J3 | J1 | | | | |
| J4 | J1 | | | | |
| J5 | J1 | | | | |
| J6 | J1 | | | | |
| L1 | Inductor, 1.0 μH | 3510003-00 | 1 | DD - 1.00 | 72259 |
| L2 | Part of PC board | | 1 | | |
| L3 | Inductor, 0.33μH | 3510007-00 | 1 | 1025-08 | 71895 |
| Q1 | PNP, GP | 4704126-00 | 2 | 2N4126 | 04713 |
| Q2 | Q1 | | | | |
| Q3 | NPN Microwave | 4710032-00 | 5 | NE02137 | 76718 |
| Q4 | Q3 | | | | |
| Q5 | PNP | 4710044-00 | 2 | MRF536 | 04713 |
| Q6 | Q3 | | | | |
| Q7 | Q3 | | | | |
| Q8 | Q5 | | | | |
| Q9 | Q3 | | | | |
| R1 | Met Ox, 51, 1/4W, 2% | 4130510-00 | 3 | C4/2%/51 | 24546 |
| R2 | Met Ox, 1K, 1/4W, 2% | 4130102-00 | 15 | C4/2%/1K | 24546 |
| R3 | Met Ox, 10K,1/4W, 2% | 4130103-00 | 5 | C4/2%/10K | 24546 |
| R4 | Met Ox, 330, 1/4W, 2% | 4130331-00 | 10 | C4/2%/330 | 24546 |
| R5 | Comp, 5.6, 1/4W, 5% | 4010569-00 | 8 | RC07GF5R6J | 24546 |
| R6 | R3 | | | | |
| R7 | Met Ox, 100, 1/4W, 2% | 4130101-00 | 5 | C4/2%/100 | 24546 |
| R8 | Met Ox, 510, 1/4W, 2% | 4130511-00 | 5 | C4/2%/510 | 24546 |

## A6 COUNT CHAIN (Continued) 2020219-01

| REF DES | DESCRIPTION | EIP NO. | UNITS PER ASSY | TYP MFR NO. | TYP FSCM NO. |
|---|---|---|---|---|---|
| R9 | R7 | | | | |
| R10 | R7 | | | | |
| R11 | R2 | | | | |
| R12 | R3 | | | | |
| R13 | R2 | | | | |
| R14 | Met Ox, 43, 1/4W, 2% | 4130430-00 | 1 | RL07S430G | 24546 |
| R15 | R1 | | | | |
| R16 | R4 | | | | |
| R17 | Met Ox, 150, 1/4W, 2% | 4130151-00 | 3 | C4/2%/150 | 24546 |
| R18 | R7 | | | | |
| R19 | Not Used | | | | |
| R20 | R4 | | | | |
| R21 | R8 | | | | |
| R22 | Met Ox, SAT 3.9K NOM | 4130392-00 | 1 | | |
| R23 | Met Ox, 620, 1/4W, 2% | 4130621-00 | 1 | C4/2%/620 | 24546 |
| R24 | Met Ox, 130, 1/4W, 2% | 4130131-00 | 2 | C4/2%/130 | 24546 |
| R25 | Met Ox, 56, 1/4W, 2% | 4130560-00 | 2 | C4/2%/56 | 24546 |
| R26 | R24 | | | | |
| R27 | Met Ox, 430, 1/4W, 2% | 4130431-00 | 1 | C4/2%/430 | 24546 |
| R28 | R5 | | | | |
| R29 | R25 | | | | |
| R30 | R4 | | | | |
| R31 | R4 | | | | |
| R32 | Met Ox, 2K, 1/4W, 2% | 4130202-00 | 2 | C4/2%/2K | 24546 |
| R33 | Met Ox, 1.5K, 1/4W, 2% | 4130152-00 | 2 | C4/2%/1.5K | 24546 |
| R34 | R2 | | | | |
| R35 | R2 | | | | |
| R36 | R2 | | | | |
| R37 | R2 | | | | |
| R38 | R5 | | | | |
| R39 | Met Ox, 39, 1/4W, 2% | 4130390-00 | 2 | C4/2%/39 | 24546 |
| R40 | R4 | | | | |
| R41 | R2 | | | | |
| R42 | Not Used | | | | |
| R43 | Met Ox, 10, 1/4W, 2% | 4130100-00 | 1 | C4/2%/10 | 24546 |
| R44 | R8 | | | | |
| R45 | Met Ox, 47, 1/4W, 2% | 4130470-00 | 2 | C4/2%/47 | 24546 |
| R46 | R39 | | | | |
| R47 | R5 | | | | |
| R48 | R2 | | | | |
| R49 | R33 | | | | |
| R50 | R2 | | | | |
| R51 | R32 | | | | |
| R52 | R8 | | | | |
| R53 | R8 | | | | |
| R54 | Not Used | | | | |
| R55 | R2 | | | | |
| R56 | Met Ox, 220, 1/4W, 2% | 4130221-00 | 1 | C4/2%/220 | 24546 |
| R57 | R7 | | | | |

## A6 COUNT CHAIN (Continued) 2020219-01

| REF DES | DESCRIPTION | EIP NO. | UNITS PER ASSY | TYP MFR NO. | TYP FSCM NO. |
|---|---|---|---|---|---|
| R58 | Met Ox, 20K, 1/4W, 2% | 4130203-00 | 4 | C4/2%/20K | 24546 |
| R59 | R58 | | | | |
| R60 | R58 | | | | |
| R61 | R58 | | | | |
| R62 | R2 | | | | |
| R63 | Met Ox, 33, 1/4W, 2% | 4130330-00 | 1 | C4/2%/33 | 24546 |
| R64 | R2 | | | | |
| R65 | Met Ox, 240, 1/4W, 2% | 4130241-00 | 2 | C4/2%/240 | 24546 |
| R66 | R65 | | | | |
| R67 | R3 | | | | |
| R68 | R4 | | | | |
| R69 | R2 | | | | |
| R70 | R3 | | | | |
| R71 | R5 | | | | |
| R72 | Not Used | | | | |
| R73 | Not Used | | | | |
| R74 | R2 | | | | |
| R75 | Not Used | | | | |
| R76 | R5 | | | | |
| R77 | R5 | | | | |
| R78 | Met Ox, 8.2, 1/4W, 2% | 4130822-00 | 1 | C4/2%/8.2K | 24546 |
| R79 | Met Ox, 750K, 1/4W, 2% | 4130754-00 | 1 | C4/2%/750K | 24546 |
| R80 | R5 | | | | |
| R81 | R1 | | | | |
| R82 | R17 | | | | |
| R83 | R4 | | | | |
| R84 | Met Ox, 270, 1/4W, 2% | 4130271-00 | 1 | C4/2%/270 | 24546 |
| R85 | R17 | | | | |
| R86 | Not Used | | | | |
| R87 | Met Ox, SAT, 2.4K NOM | 4010242-00 | 1 | | |
| R88 | R4 | | | | |
| R89 | R4 | | | | |
| R90 | R45 | | | | |
| R91 | Met Ox, 82, 1/4W, 2% | 4130820-00 | 2 | C4/2%/82 | 24546 |
| R92 | R91 | | | | |
| R93 | Met Ox, 300, 1/4W, 2% | 4130301-00 | 1 | C4/2%/300 | 24546 |
| R94 | Met Ox, 18, 1/4W, 2% | 4130180-00 | 1 | C4/2%/18 | 24546 |
| RN1 | Ntwk, 7X, 330 | 4170010-00 | 2 | 784-1-R330 | 80740 |
| RN2 | RN1 | | | | |
| RN3 | Ntwk, 5X, 330 | 4170012-00 | 1 | 783-1-R330 | 80740 |
| RN4 | Ntwk, 7X, 10K | 4170004-00 | 1 | 784-1-R10K | 00740 |
| TPI-10 | Conn, P.C. pin .040 D | 2620032-00 | 9 | 460-2970-02-03 | 71279 |
| U1 | VHF/UHF ÷ 4 Prescaler | 3043199-00 | 1 | CA3199E | 02735 |
| U2 | Triple-Line Rcvr | 3118116-00 | 2 | MC10H116P | 04713 |
| U3 | U2 | | | | |
| U4 | Triple-Line Rcvr | 3110216-00 | 2 | MC10216L | 04713 |

## A6 COUNT CHAIN (Continued) 2020219-01

| REF DES | DESCRIPTION | EIP NO. | UNITS PER ASSY | TYP MFR NO. | TYP FSCM NO. |
|---|---|---|---|---|---|
| U5 | Hex Inverter | 3007406-00 | 1 | DM7406N | 27014 |
| U6 | Triple 2-3-2 In OR/NOR | 3118105-00 | 1 | MC10H105P | 04713 |
| U7 | Dec counter | 3018634-00 | 1 | SP8634B | 58317 |
| U8 | U4 | | | | |
| U9 | Op Amp, Buffer | 3040308-00 | 3 | LM308AN | 27014 |
| U10 | Dig. Quad Translator | 3110125-00 | 1 | MC10125L | 04713 |
| U11 | Ctr, 4-bit Decade Direct | 3084160-00 | 1 | SN74LS160AN | 01295 |
| U12 | Ctr, 6-Decade Up, PMOS | 3057031-00 | 1 | LS7031 | 95035 |
| U13 | PIA to MC6800 | 3086820-00 | 1 | MC6820P/6821P | 04713 |
| U14 | DAC, 8-bit, 1/2 LSB, CMOS | 3057524-00 | 1 | AD7524JN | 01884 |
| U15 | U9 | | | | |
| U16 | U9 | | | | |
| U17 | Timer | 3040555-00 | 1 | NE555V | 18324 |

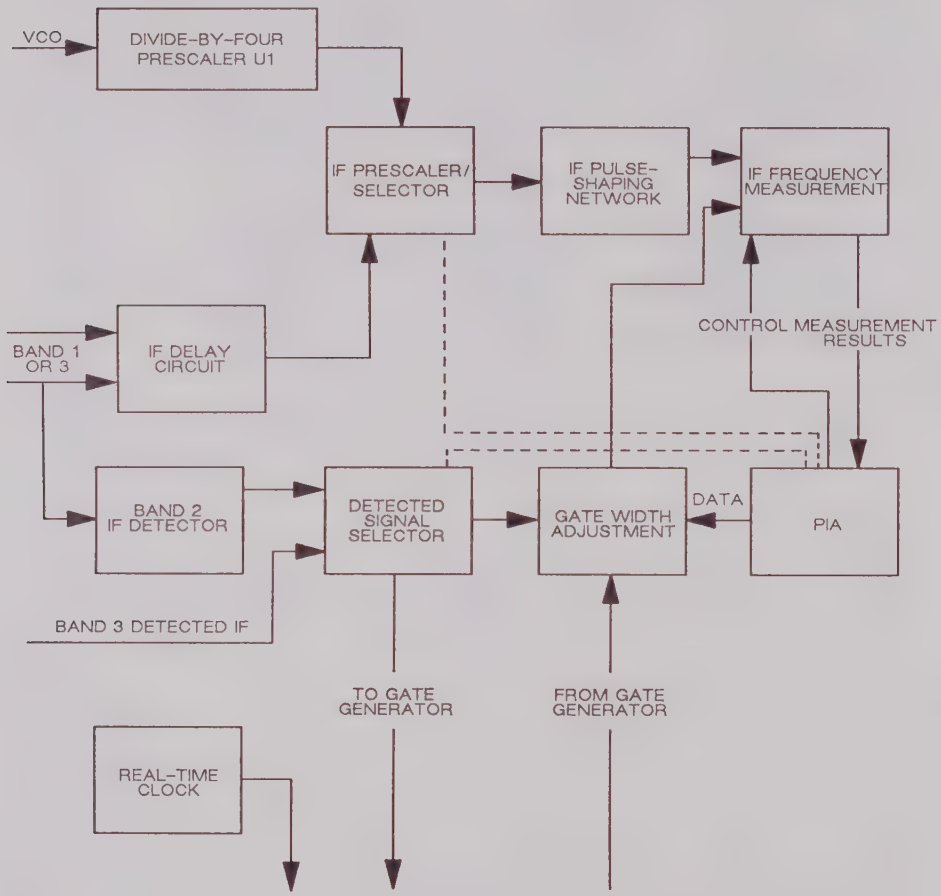



Figure 86-1. Functional Block Diagram, Count Chain

## A7 GATE GENERATOR (2020217-01)

The Gate Generator assembly generates the gate signal for frequency, pulse width, and pulse period measurements. In the frequency mode, it controls the time interval needed for the required resolution.

The Gate Generator assembly consists of the following functional blocks:

- 10-MHz Reference Oscillator
- 80-MHz Phase Lock Loop (PLL) Source
- Frequency Gate Processor
- Parameter Gate Processor
- Accumulator
- Reject Gate Circuit
- Loss-of-Lock Detector

Control and timing of the Gate Generator board signals are managed by the microprocessor through a peripheral interface adapter (PIA).

### SIGNAL PATH

The gate signal input from the Count Chain board (A6) is applied to the Reject Gate circuit, which partially or completely suppresses the gate signal if (1) the gate signal arrives in less than 200 ns from the trailing edge of the preceding gate (thus eliminating the possibility of triggering on noise or (2) it is prohibited by an active inhibit signal.

Next, the gate signal is distributed to the Parameter Gate Processor, the Frequency Gate Processor, and a buffered output. The Parameter Gate Processor puts out two pulses that indicate the beginning and the end of the signal. The Frequency Gate Processor shortens the leading edge of the gate signal so the gate signal input to the IF Frequency Measurement on the Count Chain board occurs at the middle of the IF pulse.

Both outputs are applied to the Accumulator. During the frequency measurement mode, the gate signal is sampled by the 80–MHz clock, so that its output gate width is a multiple of 12.5–ns time intervals. The output is divided between the Count Chain board and the Accumulator. The Accumulator counts the clock for one or more gate periods and terminates the current measurement cycle whenever it accumulates the total gate time necessary to achieve the requested resolution.

In the parameter measurement mode, the output of the Accumulator is equal to the width or the period of the input pulse. It is applied only to the Count Chain board. In this mode, the clock is shut off and the Accumulator is disconnected. In both modes, the gate has a third buffered output at the rear panel of the counter.

The 80–MHz clock is provided by a Phase Locked Source that receives a 10–MHz reference signal from the 10–MHz Reference Clock. This 10–MHz clock can be the internal crystal oscillator or an external source provided through the rear panel. The 10–MHz reference is also routed to the Converter Control and to the rear panel.

## 10-MHZ REFERENCE OSCILLATOR

The 10-MHz reference oscillator is the time base for the counter. It uses for a reference either an internal 10-MHz TCXO oscillator or an external reference source at rear panel connector J3. The operator uses the INT/EXT switch on the rear panel to select the required reference source. The selection is input from U18 (PIA) pin 2 to pins 5 and 8 of dual comparator U25. A low TTL logic level from U18 means the TCXO input is selected. U25 squares the sine wave input and delivers TTL output levels through U24C as a frequency reference to two PLL circuits: to pin 1 of U8 (the 80–MHz PLL), and through connector J4 to the Converter Control board. When an internal reference source is chosen, this signal is also available at the rear panel through U23C, Q6, and J3.

When an external reference is used, pin 4 of U25 is high and causes Q6 to be off, so that the external 10-MHz signal reaches U25 pin 12 through J3, a two-way (input-output) connector.

## 80-MHz PHASE-LOCKED LOOP

This PLL circuit provides an accurate 80-Mhz clock for the Accumulator block. The voltage controlled oscillator (VCO) consists of U1 and the varactor CR1. The VCO delivers its output to a divide-by 8 consisting of U13 and U14. This 10-MHz ECL output is ac coupled through C11 and translated to TTL levels by Q5. The phase detector U8 compares this signal (applied to pin 3) with the 10-MHz reference (pin 1) and generates a dc signal proportional to the phase difference. Deviation from 80-MHz causes voltage change at the VCO input in a direction that will return the frequency to 80- MHz. The output is applied to the Accumulator block via a switch during frequency measurement only. The switch consists of pin 4 of U4, which serves as an input, pin 3 of U4, which acts as an output, and pin 5 of U4, which is the control. In parameter measurement mode, pin 5 of U4 is high and shuts off the switch.

## FREQUENCY GATE PROCESSOR

The Frequency Gate Processor block is enabled when the pulse width and pulse period lines are both low. The Frequency Gate Processor receives a gate signal, an inverted pulse, from U9A pin 7 in the Reject Gate Circuit block. It then generates a gate the width of which is a multiple of 12.5 ns time intervals. This gate is shortened by approximately 30 ns from the original gate in the following manner: a capacitor to ground, C14, slows the fall time of the inverted gate signal without greatly affecting the rise time.

The signal is squared up again by a Schmitt trigger consisting of U15, R26, and R27. After passing through U9B, which is enabled by its other input being low, the gate signal reaches pin 7 of the gate flip-flop U11A. This is a fast ECL D flip-flop. This clock, at pin 9, comes from the 80-MHz PLL Source through U4A, provided the enable signal at pin 5 is low.

When the gate signal reaches the input of the gate flip-flop, the gate flip-flop is triggered by the next 80—MHz clock pulse. When the gate period ends or when the accumulator is full (U9C pin 14 is high), the next 80—MHz clock pulse turns the gate flip-flop back to the preceding state. The gate flip-flop puts out the gate signal to the Accumulator, at U11B pin 11, and to the Count Chain board on differential lines through U10C to pins 6 and 36 of the edge connector. The reset signal from U18 pin 10 is applied to U11A pin 5 from U12C pin 2 and causes the gate flip-flop U11A to be set at the beginning of the measurement cycle.

## PARAMETER GATE PROCESSOR

The purpose of this block is to put out to the Count Chain board a gate signal equal to the pulse width or the pulse period of the input signal. The Parameter Gate Processor gets its input from the Reject Gate Circuit and shares its output with U11A and U10A in the Gate Frequency Processor block. During the parameter measurement mode, the gate flip-flop U11A is used as a set-reset flip-flop; during frequency measurement,it is used as a D flip-flop.

The Parameter Gate Processor is enabled only when pulse width or pulse period measurement is selected. The gate signal is input at the junction of U3C pin 6 and U6A pin 6. U3 is an inverter used during pulse width measurement and enabled at pin 7 when the pulse width line is low. U6 functions as a divide-by-two counter (pin 3 is connected to pin 7). It is a positive edge triggered flip-flop that is enabled at pin 4 (reset) when the pulse-period line is low. U6 divides the frequency of the pulse-train by two, forming a square wave signal with its width equal to the original gate period. The signal at U3B pin 13 is a pulse whose width is equal to either the pulse width or the pulse period, depending on the selected parameter.

The circuit consisting of U7, U3B, U12A, and U12B is a pulse-forming network. It has input at U3B pin 13 and puts out two very short pulses on two different lines. The pulse input to U12 pin 3 marks the beginning of the pulse or period gate signal; the pulse input to U12 pin 15 points at the termination of the pulse or period gate. These signals serve as the set-reset signal to the input of U11A.

Before the measurement cycle begins, the flip-flop U11 must be reset. The flip-flop is reset by the board reset signal provided by U18 pin 10 through U23A, U2A, and U12C. The 80-MHz clock at U11A pin 9 that exists during the frequency mode is inhibited by a high logic signal at U4A pin 5.

Since U11A is in the set state, only a short pulse on the reset line (pointing to the leading edge of the pulse) at pin 4 switches its state, and the next short pulse on the set line, pin 5, returns it to the original state. The negative-going change on U11 pin 2 and pin 11 causes U11B to switch states and terminate this measurement cycle by placing a high logic signal at U3B pin 12. The gate signal at U11A pin 3 is delivered to the Count Chain board through U10C and pin 6 and 36 at the edge connector.

## ACCUMULATOR

The Accumulator is a high-speed binary up-counter. It counts the 80-MHz clock during the measurement cycle and stops count when its state is equal to a preset value. This value is one of five predefined maximum clock counts that the 80-MHz clock translates to total gate time of 0.1 μs, 1 μs, 10 μs, 100 μs, or 1 ms.

The Accumulator input comes from the 80-MHz clock at U11B pin 9. It has two outputs. The first, at U18 pin 12, tells the microprocessor that the measurement is over. The second output, at U9C pin 14, is an inhibit signal to the gate flip-flop, pin 7 (wire-ORed with U9B), which delivers the gate signal. The Accumulator counts only when U11B pin 13 (the clock enable) is low. The control lines of the Accumulator are the reset and gate time lines.

There are five phases of accumulator operation:

1. **Pre-measurement.** No gate signal is present. The gate flip-flop input D, U11A pin 7, is high. As a result, its Q output is high and the Accumulator is disabled.
2. **Beginning of the gate.** Input D , U11A pin 7, of the gate flip-flop changes state to low. The next 80—MHz clock signal triggers the gate flip-flop, forcing the Q output to change to low level. This enables the Accumulator. Because of the inherent delay of this IC, the Accumulator does not count this clock.
3. **Measurement.** The Accumulator begins count on the next clock and continues until it is disabled again at the enable input.
4. **End of the gate.** The gate flip-flop D, U11A pin 7, input changes state to high. On the next clock, its Q output follows the input and disables the Accumulator. Because of the inherent delay of this IC, the Accumulator counts this clock.

During pulse measurement, phases 2, 3, and 4 repeat until the sum of the total gate time approaches that of the preset gate time.

5. **End of Measurement.** After the nth count, the Accumulator inhibit output (U9C pin 14) issues a high signal to the wired-OR junction of the D input of the gate flip-flop. On the next clock, the gate flip-flop outputs a change of state (if it is not in CW, the change occurs at the middle of the current gate), preventing continuation of measurement.

The Accumulator comprises a divide-by-eight ECL counter (U11B, U5, and U6B) followed by four TTL-level decade counters (U19 and U21). The count capacity of this group is 80,000 clock pulses, which at a 80-MHz (12.5 ns) clock rate is 1 ms total. The last three decade counters (U19B, U21A, and U21B) may be removed from the string to permit the shorter gate times mentioned previously. This is done by putting a high level on the set line of the decade counter (pin 4 or 12). In addition, a divide-by-four unit (U22), which may be switched into or out of the chain, is included between the binary and the decade counter. The divide-by-four circuit is included when the counter is operating in Band 1 or 3 to increase the gate time by a factor of four. The output of those bands is prescaled by four, so the gate time must be extended to cause the counter to read the input frequency directly. The control is done by pin 7 of the PIA. In Band 2, the divide-by-four circuit is disabled and the gate U23B provides a path for the input signal around the stage.

A coincidence detector (U20) produces a low output when all the decade counters are in state 9 and the divide-by-four is in state 3. A second coincidence detector (U4B) produces a high level output when U5A, U5B, and U6B are in the 1 position. A third coincidence detector (U9C) produces the inhibit signal of the Accumulator. It uses the outputs of the two previous coincidence detectors, U20 and U4B, to produce a coincidence after n clock pulses. A fourth coincidence detector (U10B) sends the end-of-measurement message to the PIA through pin 7 and prevents any further counting by putting a high level on the set pin 12 of U11B.

It is important to remember that the gate signal itself consists of n+1 clock pulses, since the first pulse is not taken into account by the Accumulator.

To repeat the measurement, a reset signal is sent by the PIA. The reset causes the coincidence detector U9C to release the inhibit. Since this occurs last in the series of Accumulator counting operations, invalid data is not generated.

## REJECT GATE CIRCUIT

This block inhibits the gate when:

1. the signal is input less than 200 ns from the trailing edge of the preceding gate (in which case it may be noise or high PRF that is out of specification and should therefore eliminated). This is implemented by U16, a D flip-flop. U16 pin 7 is driven high by R36 and R35. When the gate signal ends, the negative transition triggers the flip-flop, forcing the Q output, pin 2, high and disabling U9A at pin 11. The capacitor C24 is charged to a high level through R39; when it reaches the appropriate voltage, after approximately 200 ns, it resets the flip-flop and enables U9A.
2. an inhibit signal is received from the rear panel.

## LOSS-OF-LOCK DETECTOR

The purpose of this circuit is to indicate to the microprocessor whether there is a signal or not. The circuit consists of a set-reset flip-flop (U16B). The microprocessor resets the flip-flop through the PIA pin 16, and after a period of time set by the MIN PRF function, checks to ascertain whether any gate signal has set it. If the flip-flop is not set, the microprocessor assumes the signal has been removed and initiates the converter search procedure.

## A7 GATE GENERATOR 2020217-01

| REF DES | DESCRIPTION | EIP NO. | UNITS PER ASSY | TYP MFR NO. | TYP FSCM NO. |
|---|---|---|---|---|---|
| C1 | Not used | | | | |
| C2 | Cer, .001μF, 5%, 50V | 2100050-00 | 1 | 1206C102J2T F | 95275 |
| C3 | Cer, 0.01μF, 10%,100V | 2150014-00 | 13 | 5020EM100RD103K | 29938 |
| C4 | X7R, 0.1μF, 10%, 50V | 2150028-00 | 9 | RC50-104KB | 51406 |
| C5 | C4 | | | | |
| C6 | Mica, 560pF, 5%, 500V | 2250036-00 | 1 | DM15CD561JCR | 84171 |
| C7 | Tant, 33μF, 10V | 2300015-00 | 5 | TAPA33M10 | 14433 |
| C8 | C4 | | | | |
| C9 | C3 | | | | |
| C10 | C4 | | | | |
| C11 | C4 | | | | |
| C12 | Not Used | | | | |
| C13 | C7 | | | | |
| C14 | Disc, Cer, SAT, 220pF, NOM | 2150047-00 | 1 | | |
| C15 | C3 | | | | |
| C16 | C3 | | | | |
| C17 | C3 | | | | |
| C18 | C3 | | | | |
| C19 | C4 | | | | |
| C20 | C3 | | | | |
| C21 | C7 | | | | |
| C22 | C3 | | | | |
| C23 | C4 | | | | |
| C24 | Mica, 100pF, 5%, 500V | 2260034-00 | 1 | CD10FD101J03 | 14655 |
| C25 | C3 | | | | |
| C26 | C3 | | | | |
| C27 | C7 | | | | |
| C28 | Tant, 10μF, 25V , 20% | 2300029-00 | 1 | DF106M25S | 76718 |
| C29 | C7 | | | | |
| C30 | C4 | | | | |
| C31 | C4 | | | | |
| C32 | C3 | | | | |
| C33 | C3 | | | | |
| C34 | C3 | | | | |
| L1 | Induct, 0.01μH | 3510001-00 | 1 | DD-0.10 | 72259 |
| CR1 | Varicap | 2710012-00 | 1 | MV109 | 04713 |
| RN1 | 7 Res, 330 ohms | 4170010-00 | 3 | 784-1-R330 | 80740 |
| RN2 | RN1 | | | | |
| RN3 | 9 Res, 330 ohms | 4170011-00 | 2 | 785-1-R330 | 80740 |
| RN4 | RN1 | | | | |
| RN5 | RN3 | | | | |
| R1 | Res, Met Ox 51, 2%, 1/4W | 4130510-00 | 2 | C4/2%/51 | 81349 |
| R2 | Met Ox, 330 1/4W, 2% | 4130331-00 | 15 | C4/2%/330 | 81349 |

## A7 GATE GENERATOR (Continued) 2020217-01

| REF DES | DESCRIPTION | EIP NO. | UNITS PER ASSY | TYP MFR NO. | TYP FSCM NO. |
|---|---|---|---|---|---|
| R3 | Met Ox, 1K, 1/4W, 2% | 4130102-00 | 10 | C4/2%/1K | 81349 |
| R4 | R3 | | | | |
| R5 | Met Ox, 36K, 1/4W, 2% | 4130363-00 | 1 | C4/2%/36K | 81349 |
| R6 | Met Ox, 150, 1/4W, 2% | 4130151-00 | 5 | C4/2%/150 | |
| R7 | Comp, 2.7, 1/4W, 5% | 4010279-00 | 3 | RC07GF2R7J | 81349 |
| R8 | Met Ox, 300, 1/4W, 2% | 4130301-00 | 3 | C4/2%/300 | 81349 |
| R9 | Met Ox, 680, 1/4W, 2% | 4130681-00 | 1 | C4/2%/680 | 81349 |
| R10 | Met Ox, 4.3K, 1/4W, 2% | 4130432-00 | 2 | C4/2%/4.3K | 81349 |
| R11 | Met Ox, 510, 1/4W, 2% | 4130511-00 | 1 | C4/2%/510 | 81349 |
| R12 | R2 | | | | |
| R13 | R7 | | | | |
| R14 | R3 | | | | |
| R15 | R6 | | | | |
| R16 | R6 | | | | |
| R17 | R8 | | | | |
| R18 | R6 | | | | |
| R19 | R2 | | | | |
| R20 | R3 | | | | |
| R21 | R6 | | | | |
| R22 | Not Used | | | | |
| R23 | R1 | | | | |
| R24 | Met Ox, 2K, 1/4W, 2% | 4130202-00 | 1 | C4/2%/2K | 81349 |
| R25 | R2 | | | | |
| R26 | Met Ox, 390, 1/4W, 2% | 4130391-00 | 2 | C4/2%/390 | 81349 |
| R27 | R26 | | | | |
| R28 | R2 | | | | |
| R29 | R2 | | | | |
| R30 | Met Ox, 100, 1/4W, 2% | 4130101-00 | 1 | C4/2%/100 | |
| R31 | R2 | | | | |
| R32 | Not Used | | | | |
| R33 | R2 | | | | |
| R34 | R2 | | | | |
| R35 | R10 | | | | |
| R36 | Met Ox, 820, 1/4W, 2% | 4130821-00 | 1 | C4/2%/820 | |
| R37 | R2 | | | | |
| R38 | R2 | | | | |
| R39 | R3 | | | | |
| R40 | R7 | | | | |
| R41 | Met Ox, 1.8K, 1/8W, 2% | 4130182-00 | 2 | C4/2%/1.8K | 81349 |
| R42 | Met Ox, 1.2K, 1/4W, 2% | 4130122-00 | 1 | C4/2%/1.2K | 81349 |
| R43 | R41 | | | | |
| R44 | R2 | | | | |
| R45 | Met Ox, 10K, 1/4W, 2% | 4130103-00 | 3 | C4/2%/10K | 81349 |
| R46 | R45 | | | | |
| R47 | R45 | | | | |
| R48 | R2 | | | | |
| R49 | R8 | | | | |
| R50 | Met Ox, 30, 1/8W, 2% | 4130300-00 | 1 | C4/2%/30 | |
| R51 | R3 | | | | |

## A7 GATE GENERATOR (Continued) 2020217-01

| REF DES | DESCRIPTION | EIP NO. | UNITS PER ASSY | TYP MFR NO. | TYP FSCM NO. |
|---|---|---|---|---|---|
| R52 | R3 | | | | |
| R53 | Met Ox, 5.1 1/4W, 5% | 4010519-00 | 2 | RC07GF5R1J | 81349 |
| R54 | R3 | | | | |
| R55 | R53 | | | | |
| R56 | R3 | | | | |
| R57 | R2 | | | | |
| R58 | R2 | | | | |
| R59 | R3 | | | | |
| Q1 | NPN, RF | 4710011-00 | 4 | 4705179 | 2N5179 |
| Q2 | Q1 | | | | |
| Q3 | Q1 | | | | |
| Q4 | Q1 | | | | |
| Q5 | NPN, GP | 4704124-00 | 1 | 2N4124 | |
| Q6 | PNP, GP | 4704126-00 | 1 | 2N4126 | |
| TP1-6 | Conn, P.C., Pin | 2620032-00 | 6 | 460-2970-02-03 | 71279 |
| J1 | Conn, Mini, P.C, Jack | 2610038-00 | 3 | 51-451-0000 | 98291 |
| J2 | J1 | | | | |
| J3 | J1 | | | | |
| J4 | 3-pin, Rt Ang, PCB | 2620132-00 | 1 | 22-05-2031 | 27264 |
| Y1 | Osc, TCXO | 2030002-00 | 1 | | |
| U1 | ECL LC VCO | 3011648-00 | 1 | MC1648P | 04713 |
| U2 | Quad Translator | 3110124-00 | 1 | MC10124L | 04713 |
| U3 | Quad 2-inp NOR Gate | 3110102-00 | 2 | MC10H102P | 04713 |
| U4 | Dgtl, Tpl OR Gate | 3110105-00 | 3 | MC10105P | 04713 |
| U5 | Dig-dual D F/F | 3110131-00 | 4 | MC10131L | 04713 |
| U6 | U5 | | | | |
| U7 | Tpl 2-inp Excl OR/NOR | 3110107-00 | 1 | MC10H107P | 04713 |
| U8 | Phase/Freq Det | 3014044-00 | 1 | MC4044L | 04713 |
| U9 | U4 | | | | |
| U10 | U4 | | | | |
| U11 | U5 | | | | |
| U12 | U3 | | | | |
| U13 | U5 | | | | |
| U14 | 10K, M-S FF | 3110231-00 | 1 | MC10231L | 04713 |
| U15 | Dgtl, Tpl Line Rcvr | 3110116-00 | 1 | MC10H116P | 04713 |
| U16 | U5 | | | | |
| U17 | Dig. Quad trans. | 3110125-00 | 1 | MC10125L | 04713 |
| U18 | PIA | 3086820-00 | 1 | MC6820P/6821P | 04713 |
| U19 | Decade Counter | 3084490-00 | 2 | SN74LS490N | 01295 |
| U20 | 13-inp Pos NAND Gate | 3070019-00 | 1 | SN74S133N | 01295 |

## A7 GATE GENERATOR (Continued) 2020217-01

| REF DES | DESCRIPTION | EIP NO. | UNITS PER ASSY | TYP MFR NO. | TYP FSCM NO. |
|---|---|---|---|---|---|
| U21 | U19 | | | | |
| U22 | Dual J-K Preset | 3087476-00 | 1 | SN74LS76A | 01295 |
| U23 | 3-inp NAND Gate | 3087411-00 | 1 | DM74LS11 | 27014 |
| U24 | Quad 2-inp Gate | 3087400-00 | 1 | DM74LS00 | 27014 |
| U25 | High Speed Dual Comp. | 3050521-00 | 1 | NE521N | |

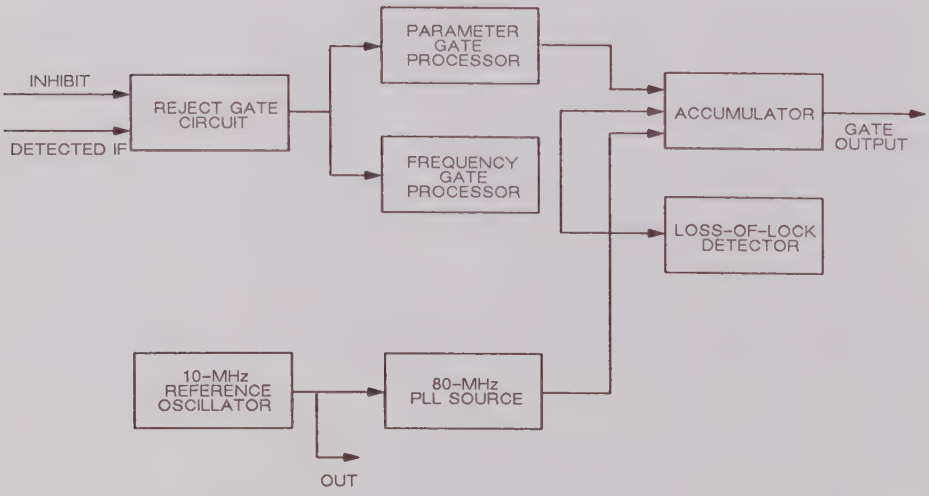



Figure 87-1. Functional Block Diagram, Gate Generator

# A8 CONVERTER CONTROL (2020200-03)

The Converter Control board performs two major functions. One of the functions is to provide a precise YIG tuning current that is controlled by the microprocessor via the Peripheral Interface Adapter (PIA) U4. The other function is to phase lock the VCO in the Microwave Converter to provide a synthesized local oscillator (LO) signal. The converter control also enables the microprocessor to control the LO power amplifier and provides the microprocessor input for the IF threshold signal.

## YIG FREQUENCY CONTROL DAC AND DRIVERS

The YIG tuning current is supplied by the YIG driver (U3, Q1, Q2, and Q3), which is controlled by the DAC. The DAC is composed of a 12-bit monolithic DAC (U2), a summing amplifier (U1), and resistors; it provides a total resolution of 14 bits. Ports 0 and 1 of the PIA (U4) are used to drive the two least significant bits of the DAC directly. A change in the least significant bit of the DAC corresponds to a YIG frequency change of 2 MHz. An analog voltage proportional to the YIG current appears across R25 and is compared to the DAC output at the summing junction of U3, with resistors R1 and R19.

The slope and offset of YIG current vs. DAC voltage are adjusted by DAC Data Correction stored in non-volatile RAM during Special Function 91 calibration.

## VCO CONTROL

The VCO control, together with the VCO, form a phase-locked-loop frequency synthesizer with a range of 400 to 505 MHz.

The output of the VCO from A10-J6 is applied to the programmable frequency divider. The programmable frequency divider is programmed by the microprocessor via PIA U7. The output of the programmable frequency divider is compared to the 50-kHz reference, derived from the 10 MHz clock, in the phase detector U14. A phase difference between the divided-down VCO and the 50 kHz reference results in an error voltage from the phase detector.

The phase detector has two output ports, a pump-up port and a pump-down port. Pump-down is U14, pin 2. Pump-down is normally high and goes low to reduce the VCO frequency. Pump-up is U18, pin 3. Pump-up is normally low and goes high to increase the VCO frequency. The outputs of the phase detector go to the charge pump, which converts them to a single tri-state output. The charge pump output is open with no pump command, sources current with pump-up, and sinks current with down. The output of the charge pump is connected to the input of the loop amplifier U19 and U17. The loop amplifier provides the proper gain and filtering to achieve the desired loop response. The output of the loop amplifier is the VCO tuning voltage. The VCO tuning voltage from A8-J2 goes to A10-J4.

## PROGRAMMABLE FREQUENCY DIVIDER

The programmable frequency divider uses a two-modulus (divide number) prescaler (U5, U6) and two programmable counters (A and B). The prescaler is used to divide the VCO frequency down to a lower frequency that can be handled by low-power Schottky TTL-programmable counters. The two-modulus prescaler permits prescaling without loss of resolution.

At the start of the programmable frequency divider cycle, the prescaler is set to divide by the larger modulus (41), and both programmable counters are loaded with their respective program numbers from the PIA. The programmable counters each decrement one count for each output pulse from the prescaler. When programmable counter B (U12, U13) reaches the count of zero, the 40/41 control flip-flop (part of U11) changes state and causes the prescaler to divide by the lower modulus (40). When programmable counter A (U8, U9, and U10) reaches the count of two, the D input of the PL period flip-flop (part of U11) goes high, so that on the count of one the flip-flop changes state. This causes both programmable counters to be reloaded with their respective program numbers and the 40/41 control flip-flop to reset the prescaler in the 41 state. The very next count causes the PL period flip-flop to reset, starting the programmable frequency divider cycle over again. The equation for the divide ratio of the programmable frequency divider $N_d$ is:

$$N_d = 40\ (N_{\text{counter A}}) + N_{\text{counter B}}$$

with the condition that :

$$N_{\text{counter B}} \text{ must not exceed } N_{\text{counter A}}$$

The weighting of the command bits is:

| | |
|---|---|
| U9 $P_1$ — 400 MHz | U10 $P_1$ — 4 MHz |
| U9 $P_0$ — 200 MHz | U10 $P_0$ — 2 MHz |
| U8 $P_3$ — 160 MHz | U13 $P_3$ — 1.6 MHz |
| U8 $P_2$ — 80 MHz | U13 $P_2$ — 0.8 MHz |
| U8 $P_1$ — 40 MHz | U13 $P_1$ — 0.4 MHz |
| U8 $P_0$ — 20 MHz | U13 $P_0$ — 0.2 MHz |
| U10 $P_3$ — 16 MHz | U12 $P_1$ — 100 kHz |
| U10 $P_2$ — 8 MHz | U12 $P_0$ — 50 kHz |

## A8 CONVERTER CONTROL 2020200-03

| REF DES | DESCRIPTION | EIP NO. | UNITS PER ASSY | TYP MFR NO. | TYP FSCM NO. |
|---|---|---|---|---|---|
| C1 | Disc, 0.005µF, 100V, 20% | 2150008-00 | 1 | TG-D50 | 56289 |
| C2 | Disc, 0.01µF, 100V, 20% | 2150003-00 | 14 | TG-S10 | 56289 |
| C3 | Cer, 0.047µF, 50V, 10% | 2150016-00 | 1 | 6123X7R473KA50 | 26654 |
| C4 | Tant, 1µF, 35V, 20% | 2300008-00 | 3 | TAPA 1.0M35 | 14433 |
| C5 | C4 | | | | |
| C6 | C2 | | | | |
| C7 | Disc, .001µF, 1KV, 20%, 100V | 2150001-00 | 4 | 5GA-D10 | 56289 |
| C8 | C4 | | | | |
| C9 | Tant, 33µF, 10%, 10V | 2300015-00 | 2 | TAPA 33M10 | 14433 |
| C10 | C7 | | | | |
| C11 | C7 | | | | |
| C12 | C7 | | | | |
| C13 | C2 | | | | |
| C14 | C2 | | | | |
| C15 | C2 | | | | |
| C16 | C2 | | | | |
| C17 | C2 | | | | |
| C18 | Tant, 10pF, 20%, 25V | 2300029-00 | 4 | DF106M25S | 72136 |
| C19 | C18 | | | | |
| C20 | C9 | | | | |
| C21 | C18 | | | | |
| C22 | C2 | | | | |
| C23 | C2 | | | | |
| C24 | C2 | | | | |
| C25 | Mono, 560pF, 5%, 100V | 2150029-00 | 2 | SR211A561JAA | 14158 |
| C26 | Tant, .47µF, 20%, 35V | 2300005-00 | 1 | TAPA-47M35 | 14433 |
| C27 | Mono, .022, 50V, 15% | 2350027-00 | 1 | 2130712050R223K | |
| C28 | C18 | | | | |
| C29 | C2 | | | | |
| C30 | Mono, 330pF, 10%, 100V | 2150030-00 | 1 | SR211A331KAA | 14158 |
| C31 | Tant, 2.2µF, 50%, 16V | 2300012-00 | 1 | TAPA 2-2M16 | 14433 |
| C32 | Mica, 82pF, 5%, 500V | 2260032-00 | 2 | CD10ED820J03 | 72136 |
| C33 | C2 | | | | |
| C34 | Mica, SAT 470 pF NOM | 2250018-00 | 1 | DM-15-471J | 72136 |
| C35 | Mica, 470 pF, 5%, 500V | 2250018-00 | 1 | DM-15-471J | 72136 |
| C36 | Mica, SAT 300 pF NOM | 2260045-00 | 1 | FC301J03 | 72135 |
| C37 | Mono, .1µF, 10%, 50V | 2150028-00 | 1 | RC50104KB | 51406 |
| C38 | C2 | | | | |
| C39 | Mono, 2200pF, 5%, 100V | 2150026-00 | 1 | SR211A22JAA | 14158 |
| C40 | C25 | | | | |
| C41 | C2 | | | | |
| C42 | C32 | | | | |
| CR1 | Hot Carrier | 2710004-00 | 1 | 5082-2835 | 28480 |
| CR2 | Zener, 56V | 2704758-00 | 1 | IN4757 | 07263 |
| CR3 | Fast Switch | 2704148-00 | 14 | IN4148 | 07263 |
| CR4 | Zener, 6.2V | 2700827-00 | 1 | IN827 | 07263 |
| CR5 | Power Rectifier | 2704001-00 | 1 | IN4001 | 07263 |
| CR6 | CR3 | | | | |

## A8 CONVERTER CONTROL (Continued) 2020200-03

| REF DES | DESCRIPTION | EIP NO. | UNITS PER ASSY | TYP MFR NO. | TYP FSCM NO. |
|---|---|---|---|---|---|
| CR7 | CR3 | | | | |
| CR8 | CR3 | | | | |
| CR9 | CR3 | | | | |
| CR10 | CR3 | | | | |
| CR11 | CR3 | | | | |
| CR12 | CR3 | | | | |
| CR13 | CR3 | | | | |
| CR14 | CR3 | | | | |
| CR15 | CR3 | | | | |
| CR16 | CR3 | | | | |
| CR17 | CR3 | | | | |
| CR18 | CR3 | | | | |
| L1 | Inductor, 100μH | 3520007-00 | 1 | 1537-76 | 99800 |
| L2 | Inductor, 1μH | 3510018-00 | 1 | 1537-12 | 99800 |
| L3 | Inductor, 4700μH | 3510017-00 | 2 | 1641-475 | 99800 |
| L4 | L3 | | | | |
| Q1 | PNP | 4710009-00 | 1 | MJE350 | 04713 |
| Q2 | PNP Amplifier | 4710018-00 | 1 | MPSL51 | 04713 |
| Q3 | NPN General Purpose | 4704124-00 | 1 | 2N4124 | 04713 |
| R1 | Prec, 7.23K, 1%, 1/10W | 4120021-00 | 1 | VAR-1/10C-6-1% 7.23K | |
| R2 | Comp, 4.7K, 5%, 1/4W | 4010472-00 | 1 | RC07GF472J | 81349 |
| R3 | Comp, 1K, 5%, 1/4W | 4010102-00 | 6 | RC076F102J | 81349 |
| R4 | Not Used | | | | |
| R5 | Met Ox, 390 ohm, 2%, 1/4W | 4130391-00 | 2 | C4/2%/390 | 24546 |
| R6 | Not Used | | | | |
| R7 | Not Used | | | | |
| R8 | R3 | | | | |
| R9 | Not Used | | | | |
| R10 | Not Used | | | | |
| R11 | Not Used | | | | |
| R12 | Not Used | | | | |
| R13 | R5 | | | | |
| R14 | Comp, 750, 5% 1/4W | 4010751-00 | 1 | RC07GF751J | 81349 |
| R15 | Comp, 820k, 5%, 1/4W | 4010824-00 | 1 | RC07GF824J | 81349 |
| R16 | R3 | | | | |
| R17 | Met Ox, 1.6K, 2%, 1/4W | 4130162-00 | 1 | C4/2%/1.6K | 24546 |
| R18 | Comp, 1.60K, 5%, 1/4W | 4010164-00 | 1 | RC07GF164J | 81349 |
| R19 | Prec, 3.01K, 1%, 1/10W | 4120020-00 | 1 | VAR-1/10C-6-1%, 3.01K | |
| R20 | Comp, 10K, 5%, 1/4W | 4010103-00 | 3 | RC07GF103J | 81349 |
| R21 | Comp, 82K, 5%, 1/4W | 4010823-00 | 1 | RC07GF823J | 81349 |
| R22 | R20 | | | | |
| R23 | R20 | | | | |
| R24 | R3 | | | | |
| R25 | Wire Wound 5, 1%, 7W | 4110003-00 | 1 | T7 (10 PPM) | 12463 |
| R26 | Comp, 2.7K, 5%, 1/4W | 4010272-00 | 1 | RC07GF272J | 81349 |
| R27 | Comp, 51, 5%, 1/4W | 4010510-00 | 2 | RC07GF510J | 81349 |
| R28 | Comp, 390, 5%, 1/4W | 4010391-00 | 3 | RC07GF391J | 81349 |

## A8 CONVERTER CONTROL (Continued) 2020200-03

| REF DES | DESCRIPTION | EIP NO. | UNITS PER ASSY | TYP MFR NO. | TYP FSCM NO. |
|---|---|---|---|---|---|
| R29 | R28 | | | | |
| R30 | R28 | | | | |
| R31 | R3 | | | | |
| R32 | Comp, 100, 5%, 1/4W | 4010101-00 | 3 | RC07GF101J | 81349 |
| R33 | R3 | | | | |
| R34 | Comp, 2.4K, 5%, 1/4W | 4010242-00 | 1 | RC07GF242J | 81349 |
| R35 | R32 | | | | |
| R36 | Comp, 220K, 5%, 1/4W | 4010224 | 1 | RC07GF224J | 81349 |
| R37 | R32 | | | | |
| R38 | Comp, S.A.T. 4.3K NOM | 4010432-00 | 1 | | |
| R39 | Comp, 2k, 5%, 1/4W | 4010202-00 | 1 | RC07GF202J | 81349 |
| R40 | R27 | | | | |
| R41 | Comp, 1.5M, 5%, 1/4W | 4010155-00 | 1 | RC07GF155J | 81349 |
| R42 | Comp, 300, 5%, 1/4W | 4010301-00 | 1 | RC07GF301J | 81349 |
| R43 | Comp, 8.2K, 5% 1/4W | 4010822-00 | 1 | RC07GF822J | 81349 |
| R44 | Comp, 51K, 5%, 1/4W | 4010513-00 | 2 | RC07GF513J | 81349 |
| R45 | Comp, 5.1K, 5%, 1/4W | 4010512-00 | 1 | RC07GF512J | 81349 |
| R46 | R44 | | | | |
| R47 | Comp, 3.3K, 5%, 1/4W | 4010332 | 1 | RC07GF332J | 81349 |
| R48 | Not Used | | | | |
| U1 | Prec, J-FET Op Amp | 3041016-00 | 1 | OP16FJ | 06665 |
| U2 | 12-Bit DAC | 3050012-00 | 1 | HS7541-1 | 0000X |
| U3 | Op Amp, Lin | 3040741-00 | 1 | LM741CN | 27014 |
| U4 | Peripheral Int Adapt | 3086820-00 | 2 | MC6820P | 04713 |
| U5 | 2-Mod Prescaler | 3112013-02 | 1 | MC12013L | 04713 |
| U6 | Digital Dual D F/F | 3110131-00 | 1 | MC10131L | 04713 |
| U7 | U4 | | | | |
| U8 | Up/Down Counter | 3084192-00 | 4 | DM74LS192 | 27014 |
| U9 | U8 | | | | |
| U10 | U8 | | | | |
| U11 | Counter Control Logic | 3112014-00 | 1 | MC12014P | 04713 |
| U12 | Up/Down Counter | 3084193-00 | 1 | DM74LS193N | 27014 |
| U13 | U8 | | | | |
| U14 | Phase Frequency Det | 3014044-00 | 1 | MC4044L | 04713 |
| U15 | Quad Dual Flip-flop | 3084175-00 | 1 | SN74LS175 | 01295 |
| U16 | Decade Counter | 3084490-00 | 1 | SN74LS490N | 01295 |
| U17 | J-FET Op Amp | 3040071-00 | 2 | TL071CP | 01295 |
| U18 | Quad 2-Inp NAND | 3087400-00 | 1 | DM74LS00 | 27014 |
| U19 | U17 | | | | |
| TP8 | Not Used | | | | |

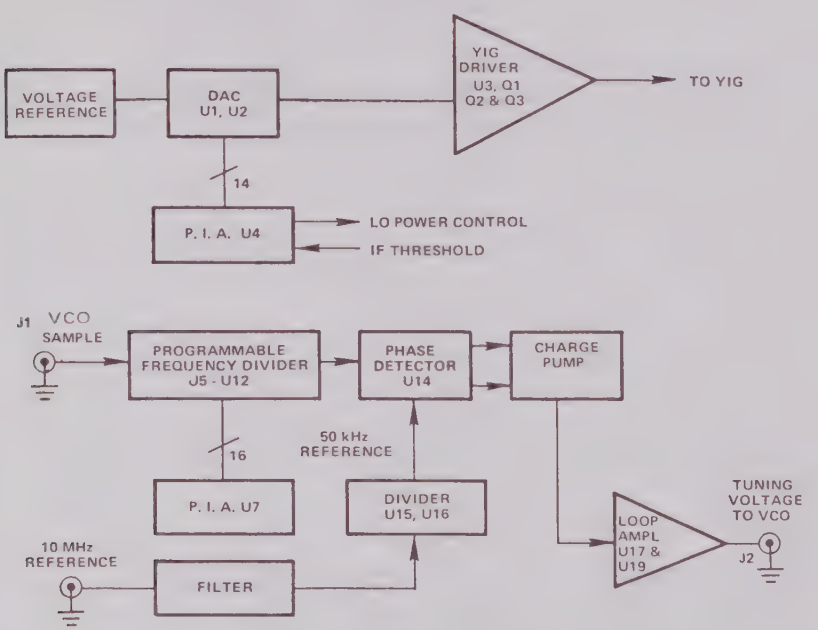



Figure 88-1. Functional Block Diagram, Converter Control

## A9 BAND 1 CONVERTER (2020224-01)

This board receives signal inputs from either the Band 1 input or the Band 3 IF. The board outputs two signals: a detected signal and the input signal divided by four. Both signals are sent to the Count Chain board.

The Band 1 Converter consists of the following functional blocks:

- Band 1 Amplifier/attenuator
- Band 1 or 3 Selector/amplifier
- RF Detector
- Divide-by-four Prescaler
- Digital Attenuator/controller

Control and timing of the Band 1 Converter board signals are performed by the microprocessor through a peripheral interface adapter (PIA).

### SIGNAL PATH

When the counter is operating in Band 1, the signal input to this board is applied to the Band 1 Amplifier/attenuator block. This block outputs the signal at a constant power level by the following process. The Loss-of-lock Detector on the Gate Generator board detects the presence of the input signal through the associated signal threshold line. The microprocessor prompts the Digital Attenuator/controller to attenuate the signal until the Loss-of-lock Detector can no longer detect it, then reduces the attenuation until the amplitude of the signal is at a level that can be detected at the signal threshold line.

When the counter is operating in Band 3, Band 1 Converter performs the same process using the Band 3 Amplifier/attenuator located in the Millimeter Wave (Band 3) Converter module.

The constant power signal from either Band 1 or Band 3 is amplified by the Selector/amplifier and then divided between the RF detector and Divide-by-four prescaler blocks.

## BAND 1 AMPLIFIER/ATTENUATOR

The Band 1 Amplifier/attenuator consists of five sub-blocks:

1. Protection circuits that protect the input from high dc voltage or high power signals. The coupling capacitor C7 eliminates high dc voltage and the 3-dB attenuator (R12, R13, and R15) and the two Schottky diodes (CR3 and CR4) protect the amplifier from high power input signals. The 3-dB attenuator also improves the input VSWR.
2. A high-pass filter (C9, L1, C10, L2, and C11) that eliminates out-of-band signals.
3. A linear amplifier (U6).
4. A switch that controls the 12 volt supply to the amplifier U6 at pin 1. This switch consists of U1A, U5, and Q3. When the output of U5 pin 14 goes low, the output of U1A, an open collector/inverter gate, goes high, and causes Q3 to turn off. When the +12-volt signal to the amplifier U6 is cut off, it causes U6 to attenuate, rather then amplify the signal, increasing the isolation between the Band 1 input and the Selector/amplifier while the counter is operating in Band 3.
5. The attenuator consists of four PIN diodes, CR6, CR7, CR8, and CR12. The control line delivers the input signal to the junction of C52 and R60. The control line voltage varies between 0 volts minimum attenuation and 8 volts maximum attenuation.

## BAND 1 OR 3 SELECTOR AMPLIFIER

This block consists of a selector that selects Band 1 or Band 3 and an amplifier.

When the counter is in Band 3, the output of U1B is low and the PIN diode CR5 in series with it conducts, presenting a low attenuation to Band 3 signals. The attenuation of signals in the Band 1 range is about 50 dB maximum.

When the counter is in Band 1, the output of U1B is high; since it is an open collector gate, it does not sink current. As a result, there is no voltage drop on R19 and the PIN diode CR5 is reverse biased, adding 20 dB of attenuation to signals in the Band 3 range.

The gain of the amplifier (U7 and U8) is about 20 dB. Since the input signal is always at the same power level, the output is about 0 dBm.

## RF DETECTOR

This block comprises a detector, a Schmitt trigger, a delay circuit, and a line driver.

The RF output from U8 reaches a detector consisting of Schottky diode CR9, resistor R64, and capacitor C25. The diode CR9 is forward biased by a current of 100 μA delivered by U10, pin 11 (the reference voltage source, VBB, of the ECL line receiver) through inductor L5. This signal is applied to the input, pin 5, of comparator U10A. The reference voltage of the comparator U10A, pin 4, is derived from the same voltage source (VBB) that feeds the detector and uses the same circuit and component values to establish this voltage. CR10 is in this case equivalent to CR9 and R40 to R37. R41, R42, U13, R54, and R51 form a unity gain amplifier with the offset generated by R53 and R50. As a result, the voltage difference between the inputs is temperature compensated.

The output of the comparator, U10A, is connected to a Schmitt trigger circuit consisting of U10B, U9A, and U9B, which gives about 3 dB of hysteresis. The Schmitt trigger circuit has two feedback loops: one feedback loop, from the output of the circuit to its input uses R63; the second, around U10, uses R24, and C44. This configuration overcomes the through put delay problem that would result in noise and oscillation during the pulse rise and fall time.

To equalize the timing of the Band 1 detector circuit to that of the Band 2 detector (on the Count Chain board), the Band 1 detected signal is delayed. C17, at the output of the Schmitt trigger circuit, delays the detected pulse on the leading edge. The capacitor slows the fall time without greatly affecting the rise time. C45, at the output of an inverter amplifier (U9C, pin 6), delays the trailing edge of the pulse and restores it to the original pulse width. If the delays are matched, the net effect is to delay the pulse.

The line driver U10C serves as a buffer and delivers its output through a differential line to the Count Chain board.

## DIVIDE-BY-FOUR PRESCALER

In order to have a frequency range at the Band 1 output that can be measured by the Count Chain board, the original input frequency must be scaled down. This is done by a divide-by-four prescaler, U11. The input impedance of U11 is a function of frequency and can significantly load the source, amplifier U8. The matching is improved by inserting a 3-dB pad (R34, R35, and R36) between U8 and U11.

In the absence of an input signal, U11 is self-oscillating; while the counter is operating in Band 2, this interference will distort the frequency measurement (the Count Chain will receive both the correct signal from Band 2 and the oscillation at the same time). To prevent oscillation, the bias point of U11 pin 2 is changed by pushing Q4 from cut-off (R33 floating) to saturation. U12, following U11, is a line driver that delivers the signal through J3 to the Count Chain board.

## DIGITAL ATTENUATOR/CONTROLLER

This block controls the attenuators on the Band 1 Converter board and the Band 3 (Millimeter Wave) Converter module. U4 is an eight-bit DAC controlled by the microprocessor through the PIA. U3 is an operational amplifier.

When the counter is operating in Band 1, U2C and U2A, parts of quad analog switch U2, are closed and U2D and U2B are open. In this case, Q2 drives the Band 1 Amplifier/attenuator and the feedback is supplied to U4, pin 16 via U2A. Q1 is turned off, setting the Band 3 attenuator to maximum attenuation (0 volts).

When the counter is operating in Band 3, U2D and U2B are closed and current is delivered to the Band 3 (Millimeter Wave) Converter. U2C is open and as a result, Q2 is saturated, which drives the Band 1 Amplifier/attenuator to maximum attenuation.

## A9 BAND 1 CONVERTER 2020224-01

| REF DES | DESCRIPTION | EIP NO. | UNITS PER ASSY | TYP MFR NO. | TYP FSCM NO. |
|---|---|---|---|---|---|
| C1 | Cer, .01μF, 100V | 2150014-00 | 11 | 5020EM100RD103K | 29938 |
| C2 | C1 | | | | |
| C3 | C1 | | | | |
| C4 | C1 | | | | |
| C5 | C1 | | | | |
| C6 | Cer, 47pF, 100V | 2150039-00 | 1 | 5018EM100RD470K | 29938 |
| C7 | Cer, 0.001μF, 100V | 2150015-00 | 20 | 5018EM1OORD102X | 29938 |
| C8 | C7 | | | | |
| C9 | Cer, 6.8pF, 100V | 2150087-00 | 3 | 5018E0100RD689K | 29938 |
| C10 | C9 | | | | |
| C11 | C9 | | | | |
| C12 | Chip, 150pF, 100V | 2100005-00 | 2 | 3BN050S151K | 26654 |
| C13 | C12 | | | | |
| C14 | Cer, 100pF 100V | 2150056-00 | 8 | 5018EM100RD101K | 29938 |
| C15 | C7 | | | | |
| C16 | Not Used | | | | |
| C17 | Cer, S.A.T. 33 pF NOM | 2150037-00 | 2 | | |
| C18 | C7 | | | | |
| C19 | C14 | | | | |
| C20 | Tant, 33μF, 10V | 2300015-00 | 2 | TAPA33M10 | 14433 |
| C21 | C14 | | | | |
| C22 | C14 | | | | |
| C23 | C7 | | | | |
| C24 | C14 | | | | |
| C25 | Cer, 4.7pF, 100V | 2150086-00 | 1 | 5018E0100RD479K | 29938 |
| C26 | C7 | | | | |
| C27 | C7 | | | | |
| C28 | C20 | | | | |
| C29 | Tant, 10μF, 25V, 20% | 2300029-00 | 2 | DF106M25S | 98104 |
| C30 | C29 | | | | |
| C31 | C1 | | | | |
| C32 | C1 | | | | |
| C33 | C14 | | | | |
| C34 | C1 | | | | |
| C35 | Cer, 33pF, 100V, 10% | 2150069-00 | 1 | 5018E0100RD33OK | 29938 |
| C36 | C1 | | | | |
| C37 | C14 | | | | |
| C38 | C7 | | | | |
| C39 | C7 | | | | |
| C40 | C14 | | | | |
| C41 | C7 | | | | |
| C42 | C7 | | | | |
| C43 | C1 | | | | |
| C44 | Cer, 22pF, 100V, 10% | 2150067-00 | 1 | 5018E0100RD22OK | 29938 |
| C45 | C17, SAT 560 pF NOM | 2150029-00 | | | |
| C46 | C7 | | | | |
| C47 | C7 | | | | |
| C48 | C7 | | | | |
| C49 | C7 | | | | |

## A9 BAND 1 CONVERTER (Continued) 2020224-01

| REF DES | DESCRIPTION | EIP NO. | UNITS PER ASSY | TYP MFR NO. | TYP FSCM NO. |
|---|---|---|---|---|---|
| C50 | C7 | | | | |
| C51 | C7 | | | | |
| C52 | C7 | | | | |
| C53 | C7 | | | | |
| C54 | C7 | | | | |
| C55 | C1 | | | | |
| CR1 | Hot Carrier | 2710004-00 | 5 | 5082-2835 | 28480 |
| CR2 | Not Used | | | | |
| CR3 | CR1 | | | | |
| CR4 | CR1 | | | | |
| CR5 | Pin | 2710024-00 | 5 | MA47123 | 96067 |
| CR6 | CR5 | | | | |
| CR7 | CR5 | | | | |
| CR8 | CR5 | | | | |
| CR9 | CR1 | | | | |
| CR10 | CR1 | | | | |
| CR11 | Zener, 5.1 V | 2705231-00 | 1 | IN5231 | 04713 |
| CR12 | CR5 | | | | |
| L1 | Part of Board | | | | |
| L2 | L1 | | | | |
| L3 | 1.2μH | 3510010-00 | 2 | 1025-22 | 99800 |
| L4 | L3 | | | | |
| L5 | 0.047μH | 3510006-00 | 1 | DD - 0.47 | 72259 |
| Q1 | NPN, GP | 4704124-00 | 2 | 2N4124 | 04713 |
| Q2 | Q1 | | | | |
| Q3 | PNP, GP | 4704126-00 | 2 | 2N4126 | 04713 |
| Q4 | Q3 | | | | |
| R1 | Not Used | | | | |
| R2 | Met Ox, 2K, 1/4W, 2% | 4130202-00 | 7 | C4/2%/2K | 24546 |
| R3 | Met Ox, 1K, 1/4W, 2% | 4130102-00 | 9 | C4/2%/1K | 24546 |
| R4 | Met Ox, 680, 1/4W, 2% | 4130681-00 | 1 | C4/2%/680 | |
| R5 | Comp, 5.6, 1/4W, 5% | 4010569-00 | 5 | C4/5%/5.6 | 24546 |
| R6 | R5 | | | | |
| R7 | Met Ox, 10K, 1/4W, 2% | 4130103-00 | 5 | C4/2%/10K | 24546 |
| R8 | Met Ox, 360, 1/4W, 2% | 4130361-00 | 1 | C4/2%,/360 | 24546 |
| R9 | R3 | | | | |
| R10 | R3 | | | | |
| R11 | R7 | | | | |
| R12 | Comp, 8.2, 1/4W, 5% | 4010829-00 | 3 | C4/5%/8.2 | 24546 |
| R13 | Met Ox, 150, 1/4W, 2% | 4130151-00 | 2 | C4/2%/150 | 24546 |
| R14 | R3 | | | | |
| R15 | R12 | | | | |
| R16 | Met Ox 33, NOM SAT | 4130030-00 | 6 | | |
| R17 | Met Ox, 20, NOM, SAT | 4130200-00 | 1 | | |
| R18 | R16 | | | | |
| R19 | R7 | | | | |

## A9 BAND 1 CONVERTER (Continued) 2020224-01

| REF DES | DESCRIPTION | EIP NO. | UNITS PER ASSY | TYP MFR NO. | TYP FSCM NO. |
|---|---|---|---|---|---|
| R20 | R3 | | | | |
| R21 | R2 | | | | |
| R22 | Met Ox, 270, 1/4W, 2% | 4130271-00 | 3 | C4/2%/270 | 24546 |
| R23 | Met Ox, 8.2K, NOM, SAT | 4130822-00 | | | |
| R24 | R3 | | | | |
| R25 | R3 | | | | |
| R26 | Met Ox, 330, 1/4W, 2% | 4130331-00 | 9 | C4/2%/330 | 24546 |
| R27 | R26 | | | | |
| R28 | R26 | | | | |
| R29 | R26 | | | | |
| R30 | Met Ox, 51, 1/4W, 2% | 4130510-00 | 1 | C4/2%/51 | 24546 |
| R31 | R7 | | | | |
| R32 | R3 | | | | |
| R33 | R7 | | | | |
| R34 | Met Ox, 47, 1/4W, 2% | 4130470-00 | 1 | C4/2%/47 | 24546 |
| R35 | R12 | | | | |
| R36 | R13 | | | | |
| R37 | R2 | | | | |
| R38 | R26 | | | | |
| R39 | R22 | | | | |
| R40 | R2 | | | | |
| R41 | Met Ox, 51K, 1/4W, 2% | 4130513-00 | 4 | C4/2%/51K | 24546 |
| R42 | R41 | | | | |
| R43 | R5 | | | | |
| R44 | R3 | | | | |
| R45 | Met Ox, 620, 1/4W, 2% | 4130621-00 | 2 | C4/2%/620 | 24546 |
| R46 | R26 | | | | |
| R47 | R45 | | | | |
| R48 | R5 | | | | |
| R49 | R26 | | | | |
| R50 | Met Ox, 82, NOM SAT | 4130820-00 | 1 | | |
| R51 | R41 | | | | |
| R52 | R5 | | | | |
| R53 | Met Ox, 8.2, 1/4W, 2% | 4130822-00 | | C4/2%/8.2 | 24546 |
| R54 | R41 | | | | |
| R55 | R26 | | | | |
| R56 | Met Ox, 24K, 1/4W, 2% | 4130243-00 | 1 | C4/2%/24K | 24546 |
| R57 | R23 | | | | |
| R58 | R2 | | | | |
| R59 | Met Ox, 12K, 1/4W, 2% | 4130123-00 | 1 | C4/2%/12K | 24546 |
| R60 | R2 | | | | |
| R61 | R26 | | | | |
| R62 | R22 | | | | |
| R63 | R2 | | | | |
| R64 | R30 | | | | |
| R65 | Met Ox, 750, 1/4W, 2% | 4130751-00 | 1 | C4/2%/750 | 24546 |
| U1 | Hex Inverter | 3007406-00 | 1 | DM7406N | 27014 |
| U2 | Analog Switch | 3034066-00 | 1 | MC14066B | 04713 |
| U3 | Op Amp buff | 3040308-00 | 2 | LM308AN | 27014 |

## A9 BAND 1 CONVERTER (Continued) 2020224-01

| REF DES | DESCRIPTION | EIP NO. | UNITS PER ASSY | TYP MFR NO. | TYP FSCM NO. |
|---|---|---|---|---|---|
| U4 | DAC, 8-Bit, 1/8 lsb, CMOS | 3057525-00 | 1 | AD7524LN | 51640 |
| U5 | PIA Periph to MC6800 | 3086820-00 | 1 | MC6820P/6821P | 04713 |
| U6 | Cascadable Amp | 3041063-00 | 3 | GPD-1003/1063 | 24539 |
| U7 | U6 | | | | |
| U8 | U6 | | | | |
| U9 | EXL 10K, Line Rcvrs | 3110116-00 | 1 | MC10H116P | 04713 |
| U10 | ECL 10KH, Line Rcvrs | 3118116-00 | 2 | MC10H116P | 04713 |
| U11 | VHF/UHFm 4 Prescaler | 3043199-00 | 1 | CA3199E | 02735 |
| U12 | U10 | | | | |
| U13 | U3 | | | | |
| J1 | Coax PC Rec Snap Nan | 2610038-00 | 3 | 51-451-0000 | 98291 |
| J2 | J1 | | | | |
| J3 | J1 | | | | |

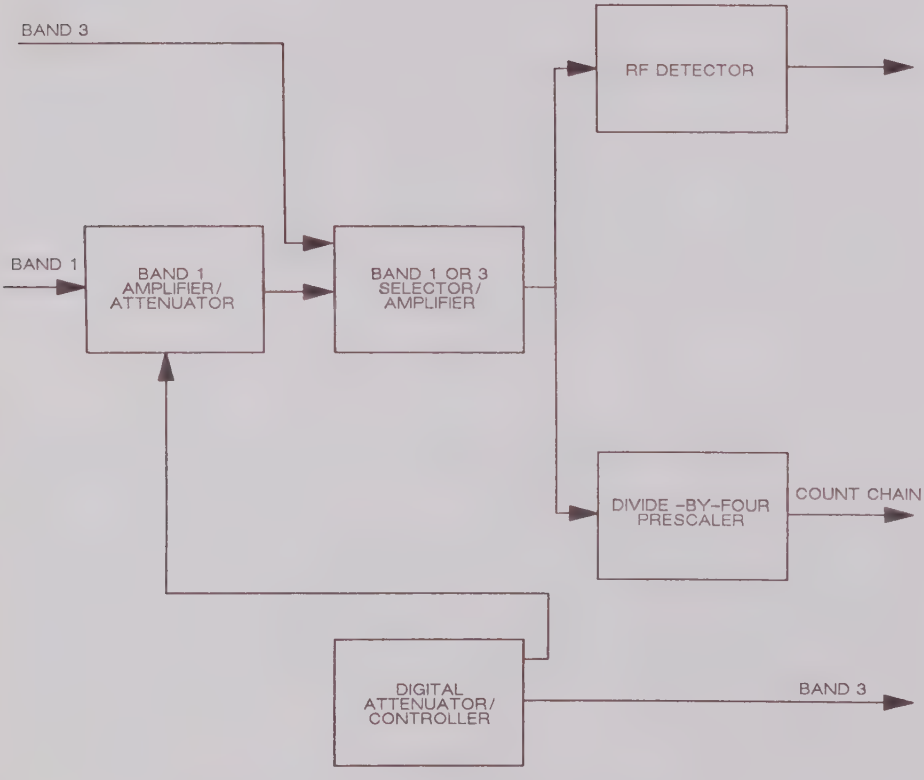



Figure 89-1. Functional Block Diagram, Band 1 Converter (Option)

# A10 BAND 2 MICROWAVE CONVERTER (2010296-01)

## GENERAL

The Band 2 Microwave Converter is a complete microwave subsystem consisting of three printed circuit assemblies: the IF/Video Amplifier, the VCO, and the VCO Buffer. It converts an input signal in the range of 0.95 GHz to 18 GHz/26.5 GHz down to an IF of 110 MHz. Down conversion is achieved in this heterodyne system by combining the input signal with a harmonic of a precisely known reference signal, $F_{VCO}$. The mixer then produces a signal, $F_{IF}$, equal to the difference between the input and reference harmonic. If this difference is close to 110 MHz, it is amplified to a level of about 0 dBm and then counted. The input signal is then determined for the equation

$$F_{IN} = NF_{VCO} \pm F_{IF}$$

$F_{VCO}$ is set by the instrument program via a phase-locked loop located on the Converter Control board (A8) and is thus known exactly.

Harmonics of the VCO are produced by the comb generator and coupled to the mixer. The frequency ranges of the VCO and IF are such that for any VCO frequency and any input frequency, only one harmonic can produce an IF frequency. The YIG filter located between the RF input and the mixer is used to determine the input frequency approximately. From this information the desired values of N, $F_{VCO}$, and mix side are determined.

### NOTE

**Due to the extensive test equipment and special processes required to test and repair this assembly, it is not recommended that any field repair be attempted. For this reason the manual does not contain detailed information on the circuitry contained in this assembly. Exchange modules are available from EIP. Please consut the factory for pricing.**

## A11 BAND 3 CONVERTER (2020238-01)

The Band 3 Millimeter Wave Converter is a heterodyne harmonic downconverter, employing millimeter wave harmonic mixers in the various waveguide bands from 26.5 to 110 GHz. These mixers are external to the instrument.

Local oscillator frequency (LO) is created by multiplying the VCO input frequency to the Millimeter Wave Converter by 12. This LO signal is channeled to the external mixer through a coaxial cable. The resulting IF signal, returning through the same cable, is separated and processed in the converter.

The major parts of the converter are the following:

- Power Amplifier
- Multiplier
- IF Amplifier

### POWER AMPLIFIER

The power amplifier consists of three bipolar transistor stages, preceded by a high-pass filter to cut down on wide-band noise entering the amplifier. The first stage is operated linearly (class A), and does not require tuning. The second and third stages are turned on by the RF power, and need to be adjusted for best performance.

### MULTIPLIER

The Multiplier, consisting of the X3 Multiplier, the X4 Multiplier, and the LO Amplifier/Diplexer, multiplies the incoming VCO frequency by 12 to supply the LO power to an external mixer. The LO amplifier doubles the output power while providing buffering between the mixer and the multiplier chain.

The IF signal, separated in the diplexer, is amplified and filtered in the variable gain IF amplifier strip.

## IF AMPLIFIER

The IF amplifier increases the amplitude of the IF signal generated by a harmonic mixer to approximately -5 dBm while suppressing all other signals, such as harmonics of the VCO, that are present at the input at levels far exceeding that of the desired IF signal.

Since the amplifier processes pulsed signals, it must always be kept in the linear operating range, regardless of the IF input level. This is done by varying the bias current of two of the amplifier stages by microprocessor control, according to output level, to keep the output level constant at approximately -5 dBm.

### NOTE

**Due to the extensive test equipment and special processes required to test and repair this assembly, it is not recommended that any field repair be attempted. For this reason the manual does not contain detailed information on the circuitry contained in this assembly. Exchange modules are available from EIP. Please consut the factory for pricing.**

# A12A1 FRONT PANEL DISPLAY and KEYBOARD (2020140-02)

The Front Panel Display and Keyboard assembly is divided into two functional sections:

- Numeric display and annunciators
- Keyboard

## NUMERIC DISPLAY AND ANNUNCIATORS

This section of the assembly contains 12 common-anode, seven-segment numeric display units (DS1-DS12), 2 green LEDs (DS37 and DS38), and 24 yellow LEDs (DS13-DS36).

The seven-segment LEDs are mounted side by side, with space between each third digit from the right. The corresponding cathode segments of the seven-segment LEDs are connected, and the drive signals come from the segment drivers Q3 through Q10. The signals to drive the digits come from the digit drivers located on the Front Panel Logic board.

The two green LEDs (DS37 and DS38) are driven by Q1 and Q2. When these LEDs light, they indicate that the GATE and CONVERTER SEARCH modes are in operation.

The yellow LEDs (DS13-DS36) are divided into three groups of eight each. The anodes of all LEDs in each group are connected. The cathode of each grouped LED is connected to one of the segment drivers (Q3 through Q10). With this arrangement, each group of annunciator lights can be regarded as similar to one seven-segment LED. The digit drives for the three groups of annunciator lights also come from the Front Panel Logic board.

## KEYBOARD

This section of the assembly contains 21 single-pole, double-throw switches. The switches are arranged in a four-row by six-column matrix, with the extra switch taking the row 4, column 7 position. The columns are connected to +5 volts through the resistor network (RN1) on the Front Panel Logic board.

The keyboard is continuously scanned. The signals scanning the keyboard are derived from the Front Panel Logic board. When the keyboard is being scanned, the four rows are grounded sequentially. When a row is grounded, and a key in that row is pressed, one of the columns will be grounded. This information is sent to the Front Panel Logic board, where key debouncing is performed.

The keyboard is continuously scanned. The signals scanning the keyboard are derived from the Front Panel Logic board (A12A2). When the keyboard is being scanned, the four rows are grounded sequentially. When a row is grounded, and a key in that row is pressed, one of the columns will be grounded. This information is sent to the Front Panel Logic board, where key debouncing is performed.

## A12A1 FRONT PANEL DISPLAY AND KEYBOARD 2020140-02

| REF DES | DESCRIPTION | EIP NO. | UNITS PER ASSY | TYP MFR NO. | TYP FSCM NO. |
|---|---|---|---|---|---|
| Q1 | PNP, Amp | 4710019-00 | 10 | MPS-D55 | 04713 |
| Q2 | Q1 | | | | |
| Q3 | Q1 | | | | |
| Q4 | Q1 | | | | |
| Q5 | Q1 | | | | |
| Q6 | Q1 | | | | |
| Q7 | Q1 | | | | |
| Q8 | Q1 | | | | |
| Q9 | Q1 | | | | |
| Q10 | Q1 | | | | |
| R1 | Comp, 4.7K, 5%, 1/4W | 4010472-00 | 2 | RC07GF472J | 81349 |
| R2 | Comp, 130, 5%, 1/4W | 4010131-00 | 2 | RC07GF131J | 81349 |
| R3 | R1 | | | | |
| R4 | R2 | | | | |
| R5 | Comp, 240, 5%, 1/4W | 4010241-00 | 8 | RC07GF241J | 81349 |
| R6 | Comp, 18, 5%, 1/4W | 4010180-00 | 8 | RC07GF180J | 81349 |
| R7 | R5 | | | | |
| R8 | R6 | | | | |
| R9 | R5 | | | | |
| R10 | R6 | | | | |
| R11 | R5 | | | | |
| R12 | R6 | | | | |
| R13 | R5 | | | | |
| R14 | R6 | | | | |
| R15 | R5 | | | | |
| R16 | R6 | | | | |
| R17 | R5 | | | | |
| R18 | R6 | | | | |
| R19 | R5 | | | | |
| R20 | R6 | | | | |
| DS1 thru DS12 | LED, Numeric, Red | 2800024-01 | 12 | TIL-312 HDSP-3108 | 28480 |
| DS13 thru DS36 | LED, Lamp, Yel 0.15 X 0.25 | 2800020-00 | 24 | MV53124 | 50522 |
| DS37 | LED, Lamp, Grn | 2800018-00 | 2 | MV5274B | 50522 |
| DS38 | DS37 | | | | |
| S1 | Switch Mon, SPDT | 4500013-00 | 21 | REK | |
| S2 | Not Used | | | | |
| S3 | Not Used | | | | |
| S4 | Not Used | | | | |
| S5 | Not Used | | | | |

## A12A1 FRONT PANEL DISPLAY AND KEYBOARD 2020140-02

| REF DES | DESCRIPTION | EIP NO. | UNITS PER ASSY | TYP MFR NO. | TYP FSCM NO. |
|---|---|---|---|---|---|
| S6 | S1 | | | | |
| S7 | S1 | | | | |
| S8 | S1 | | | | |
| S9 | S1 | | | | |
| S10 | S1 | | | | |
| S11 | S1 | | | | |
| S12 | S1 | | | | |
| S13 | S1 | | | | |
| S14 | S1 | | | | |
| S15 | S1 | | | | |
| S16 | S1 | | | | |
| S17 | S1 | | | | |
| S18 | S1 | | | | |
| S19 | S1 | | | | |
| S20 | S1 | | | | |
| S21 | S1 | | | | |
| S22 | S1 | | | | |
| S23 | S1 | | | | |
| S24 | S1 | | | | |
| S25 | S1 | | | | |
| P1 | 9-Pin Recept | 2620065-00 | 1 | 22 - 14 - 2094 | 0000A |
| P2 | 17-Pin Recept | 2620067-00 | 1 | 22 - 14 - 2171 | 0000A |
| P3 | 13-Pin Recept | 2620066-00 | 1 | | |

# A12A2 FRONT PANEL LOGIC (2020191-01)

The Front Panel Logic assembly contains logic circuitry for control of two functions:

- Display control
- Keyboard control

The +5 volt power supply to the front panel assemblies is regulated by a voltage regulator that is located behind the Front Panel Logic board. For heat-sinking purposes, this voltage regulator is mounted on the chassis as shown in Front Panel Logic Schematic Diagram.

## DISPLAY CONTROL

The signals input to the twelve 7-segment LEDs and the three groups of annunciator lights on the Front Panel Display are multiplexed. To turn on a particular segment in a digit, both the digit driver for that digit and the segment driver for that segment must be on.

The display logic is in constant operation in either the self-scan mode or the memory update mode.

## SELF-SCAN MODE

This is the normal operating mode. In this mode, the display scan clock is clocking the display counter (U6). The state of the display counter determines which digit will be turned on.

The state of the display counter is decoded by a 4-to-16-line multiplexer (U2), and the appropriate digit driver is turned on. At this time, the display memory (U7 and U8) is read, and the on/off information (stored in the display memory for that specific digit) turns the segment drivers on the Front Panel Display board on or off.

The display intensity is controlled by varying the duty cycle of the multiplexer. This is done by varying the resistance of the potentiometer (R4) which, in turn, varies the length of time the decoder (U2) and the display memories (U7, U8) are disabled between each scan clock cycle.

At the start of each gate operation, the GATE LED control is triggered, and the GATE LED lights for the length of the gate time.

## MEMORY UPDATE MODE

In this mode, the display scan/$\overline{\text{update}}$ control line (PA4) is set to logic 0, disabling the multiplexer. The microprocessor-controlled clock (PA1) is used to clock the display counter (U6).

The microprocessor sets the clear/load control line (PA5) to logic 1 and clocks the clock input of U6, which clears the display counter and updates the display memory (U7 and U8). Update mode timing is illustrated in Figure 812A2-1.

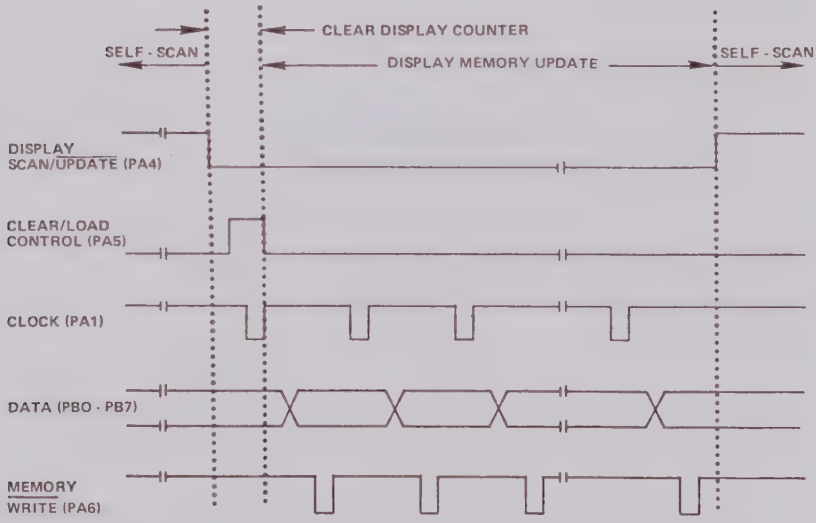



Figure 812A2-1. Update Mode Sequence

## KEYBOARD CONTROL

When the keyboard is not being read by the microprocessor, the keyboard read/$\overline{\text{scan}}$ control line (PA0) is at logic 0. All the outputs of the shift register are at logic 0. If no key on the keyboard is pressed, all the inputs to the 8-input NAND gate (U13) are at logic 1 level. When a key is pressed, the column containing that key is grounded. The output of U13 goes to logic 1 and C7 (in the debounce circit) starts to discharge. When the voltage across C7 reaches approximately +0.7 volts above ground, the debounce circuit will trigger the interrupt input of the PIA (U11, pin 18), indicating that a key is being pressed.

## READ KEYBOARD

When the microprocessor needs to read the keyboard, a logic 1 signal is put on the keyboard read/$\overline{\text{scan}}$ control line (PA0). This enables the data buffer (U9). A 0111 is then loaded into the shift register (U3) by putting a logic 1 on the clear/load control line (PA5) and clocking the clock input of U3. The logic 0 at the output of the shift register (U3) is shifted through the shift register once. The microprocessor reads the keyboard row and column information with the logic 0 at each of the four outputs of U3 to determine the coordinate of the key pressed. After the keyboard is read, the keyboard read/scan line is returned to logic 0.

## A12A2 FRONT PANEL LOGIC 2020191-02

| REF DES | DESCRIPTION | EIP NO. | UNITS PER ASSY | TYP MFR NO. | TYP FSCM NO. |
|---|---|---|---|---|---|
| C1 | Tant, 0.1µF, 10%, 35V | 2300020-00 | 1 | TAPA .10M35 | 14433 |
| C2 | Cer., .002µF, 20%, 1KV | 2150005-00 | 2 | TG-S20 | 56289 |
| C3 | C2 | | | | |
| C4 | Not Used | | | | |
| C5 | Tant, 47µF, 20%, 16V | 2300025-00 | 1 | TAPA 47M16 | 14433 |
| C6 | Tant, 2.2 µF, 20%, 16V | 2300012-00 | 1 | TAPA 2.2M16 | 14433 |
| C7 | Tant, 22µF, 20%, 16V | 2300030-00 | 1 | TAPA 22M16 | 14433 |
| C8 | Tant, .33µF, 20%, 35V | 2300031-00 | 1 | TAPA .33M16 | 14433 |
| C9 | Tant, 33µF, 20%, 10V | 2300015-00 | 1 | TAPA 33M16 | 14433 |
| C10 | Cer., .01µF, 20%, 100V | 2150003-00 | 6 | TG-S10 | 56289 |
| C11 | C10 | | | | |
| C12 | C10 | | | | |
| C13 | C10 | | | | |
| C14 | C10 | | | | |
| C15 | C10 | | | | |
| CR1 | Fast Switch | 2704148-00 | 1 | 1N4148 | 07263 |
| J1 | 9 Pin Male | 2620062-00 | 1 | 22-03-2091 | 0000B |
| J2 | 17 Pin Male | 2620064-00 | 1 | 22-03-2171 | 0000B |
| J3 | 13 Pin Male | 2620063-00 | 1 | 22-03-2131 | 0000B |
| J4 | 4 Pin, Fr.Lock | 2620068-00 | 1 | 640456-4 | 74868 |
| J5 | 3 Pin | 2620121-00 | 1 | 640456-3 | 74868 |
| P2 | 26 Pin, Right Angle | 2620131-00 | 1 | 3493-1002 | 76381 |
| Q1 | PNP, Power | 4710027-00 | 15 | MPS - D54 | 04713 |
| Q2 | Q1 | | | | |
| Q3 | Q1 | | | | |
| Q4 | Q1 | | | | |
| Q5 | Q1 | | | | |
| Q6 | Q1 | | | | |
| Q7 | Q1 | | | | |
| Q8 | Q1 | | | | |
| Q9 | Q1 | | | | |
| Q10 | Q1 | | | | |
| Q11 | Q1 | | | | |
| Q12 | Q1 | | | | |
| Q13 | Q1 | | | | |
| Q14 | Q1 | | | | |
| Q15 | Q1 | | | | |
| Q16 | NPN, General Purpose | 4704124-00 | 2 | 2N4124 | 04713 |
| Q17 | Q16 | | | | |

## A12A2 FRONT PANEL LOGIC (Continued) 2020191-02

| REF DES | DESCRIPTION | EIP NO. | UNITS PER ASSY | TYP MFR NO. | TYP FSCM NO. |
|---|---|---|---|---|---|
| R1 | Comp, 10K, 5%, 1/4W | 4010103-00 | 2 | RC07GF103J | 81349 |
| R2 | Comp, 220, 5%, 1/4W | 4010221-00 | 1 | RC07GF221J | 81349 |
| R3 | Comp, 75K, 5%, 1/4W | 4010753-00 | 1 | RC07GF753J | 81349 |
| R4 | Variable, Cer., 200K | 4250022-00 | 1 | 72XR200 | 73138 |
| R5 | Comp, 120K, 5%, 1/4W | 4010124-00 | 1 | RC07GF124J | 81349 |
| R6 | Comp, 2.4K, 5%, 1/4W | 4010242-00 | 1 | RC07GF242J | 81349 |
| R7 | Comp, 1K, 5%, 1/4W | 4010102-00 | 15 | RC07GF102J | 81349 |
| R8 | R7 | | | | |
| R9 | R7 | | | | |
| R10 | R7 | | | | |
| R11 | R7 | | | | |
| R12 | R7 | | | | |
| R13 | R7 | | | | |
| R14 | R7 | | | | |
| R15 | R7 | | | | |
| R16 | R7 | | | | |
| R17 | R7 | | | | |
| R18 | R7 | | | | |
| R19 | R7 | | | | |
| R20 | R7 | | | | |
| R21 | R7 | | | | |
| R22 | Not Used | | | | |
| R23 | Comp, 15K, 5%, 1/4W | 4010153-00 | 1 | RC07GF153J | 81349 |
| R24 | Comp, 390, 5%, 1/4W | 4010391-00 | 1 | RC07GF391J | 81349 |
| R25 | Comp, 200, 5%, 1/4W | 4010201-00 | 1 | RC07GF201J | 81349 |
| R26 | Comp, 1K NOM SAT | 4010102-00 | 1 | | |
| R27 | R1 | | | | |
| R28 | Not Used | | | | |
| R29 | Comp, 2.2K, 5%, 1/4W | 4010222-00 | 1 | RC07GF222J | 81349 |
| R30 | Not Used | | | | |
| R31 | Comp, 27K, 5%, 1/4W | 4010273-00 | 1 | RC07GF273J | 81349 |
| R32 | Comp, 39K, 5%, 1/4W | 4010393-00 | 3 | RC07GF393J | 81349 |
| R33 | R32 | | | | |
| R34 | R32 | | | | |
| RN1 | Network, 9 x 10K, 0.2W, 2% | 4170003-00 | 2 | 785-1-R10K | 32997 |
| RN2 | RN1 | | | | |
| RN3 | Network, 7 x 10K, 0.3W, 2% | 4170004-00 | 1 | 784-1-R10K | 32997 |
| TP1 | 0.040D Pin | 2620032-00 | 9 | 460-2970-02-03 | 71279 |
| TP2 | TP1 | | | | |
| TP3 | PT1 | | | | |
| TP4 | TP1 | | | | |
| TP5 | TP1 | | | | |
| TP6 | TP1 | | | | |
| TP7 | Not Used | | | | |
| TP8 | TP1 | | | | |
| TP9 | TP1 | | | | |

## A12A2 FRONT PANEL LOGIC (Continued) 2020191-02

| REF DES | DESCRIPTION | EIP NO. | UNITS PER ASSY | TYP MFR NO. | TYP FSCM NO. |
|---|---|---|---|---|---|
| TP10 TP1 | | | | | |
| U1 | TTL/Monostable, MV | 3084123-00 | 2 | DM74LS123N | 0000X |
| U2 | 4-16 Line Decoder | 3074154-00 | 1 | DM74154N | 0000X |
| U3 | 4-Bit Shift Register | 3084195-00 | 1 | DM74LS195N | 0000X |
| U4 | AND/OR Invert Gates | 3087451-00 | 1 | SN74LS51N | 01295 |
| U5 | Quad, 2-Inp NAND Gate | 3084132-00 | 1 | DM74LS132N | 0000X |
| U6 | Binary Counter | 3084163-00 | 1 | SN74LS163 | 01295 |
| U7 | Bipolar RAM | 3057489-00 | 2 | DM74LS189 | 0000X |
| U8 | U7 | | | | |
| U9 | Oct Bus Trans | 3084244-00 | 1 | SN74LS244N | 01295 |
| U10 | U1 | | | | |
| U11 | Periph. Int Adapt. | 3086821-00 | 1 | MC68B21P | 04713 |
| U12 | Hex Inverter | 3087414-00 | 1 | SN74LS14N | 01295 |
| U13 | 8-Inp NAND Gate | 3087430-00 | 1 | DM74LS30N | 0000X |

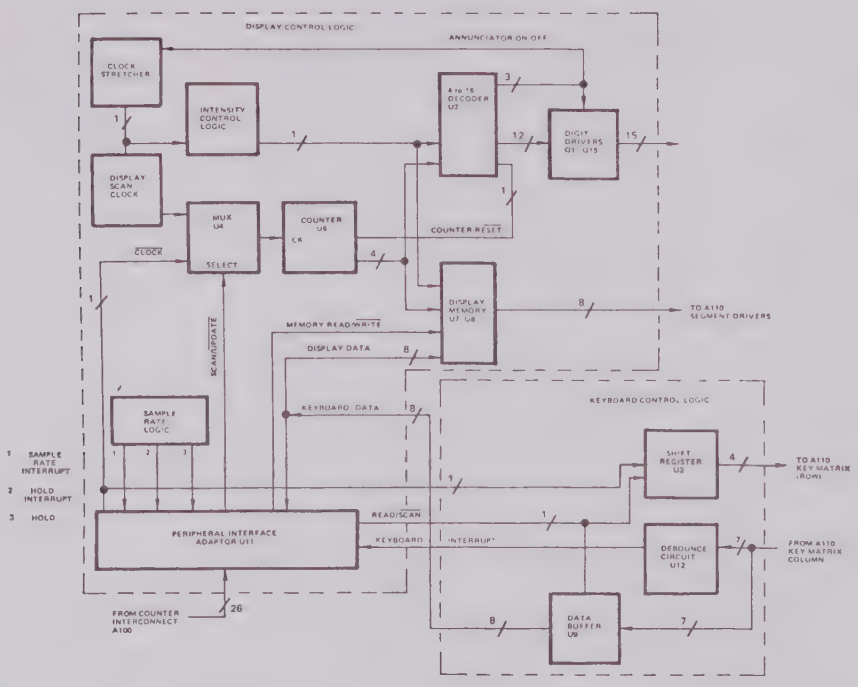



Figure 812A2-2. Functional Block Diagram, Front Panel Logic

# Appendix A
# List of Manufacturers

| FSCM | MANUFACTURER |
|---|---|
| 0000X | Any Manufacturer of this product. |
| 00656 | Aerovox Inc., New Bedford, MA 02741 |
| 00779 | Amp, Inc, Harrisburg, PA 17105 |
| 00809 | Croven Ltd., Whitby, Ontario, Canada |
| 01121 | Allen-Bradley Co., South Milwaukee, WI 53204 |
| 01295 | Texas Instruments Inc., Dallas, TX 75222 |
| 02088 | Kelvin Electric, Fajardo, PR 00648 |
| 02660 | Amphenol Connector Div., Bunker Ramo Corp., Broadview, IL 60153 |
| 02735 | Solid State Div., RCA Corp., Somerville, NJ 08876 |
| 04618 | American Pamcor Inc., Paoli, PA 19301 |
| 04713 | Motorola Inc., Semiconductor Div., Phoenix, AZ 85008 |
| 06665 | Precision Monolithic Inc., Santa Clara, CA 95050 |
| 07263 | Fairchild Semiconductor, Mountain View, CA 94040 |
| 08717 | Sloan Company, Sun Valley, CA 91352 |
| 09353 | C & K Components Inc., Watertown, MA 02172 |
| 11236 | CTS of Berne Inc., Berne, IN 46711 |
| 11237 | CTS, Keen, Paso Robles, CA 93446 |
| 12463 | Optronics Mfg., Omaha, NE 68106 |
| 14158 | AVX Filters, San Diego, CA 92131 |
| 14298 | American Components Inc., Conshohocken, PA 19428 |
| 14433 | ITT Semiconductor Div., West Palm Beach, FI 33401 |
| 14455 | Quality Hardware Mfg. Co., Hawthorn, CA 90250 |
| 14655 | Cornell Dubilier, Newark, NJ 07101 |
| 18324 | Signetics Corp., Sunnyvale, Ca 94086 |
| 23880 | Stanford Applied Engineering Inc., Santa Clara, CA 95050 |
| 23036 | Pamotor Inc., Burlingame, CA 94010 |
| 24539 | Avantek, Santa Clara, CA 95051 |
| 24546 | Corning Glass Works, Bradford, PA 16701 |
| 26654 | Varadyne Ind., Santa Monica, CA 90404 |
| 27014 | National Semiconductor Corp., Santa Clara, CA 95051 |
| 27264 | Molex, Inc, Lisle, IL 60532 |
| 28480 | Hewlett-Packard Co., Palo Alto, CA 94304 |
| 29938 | Emcon Machine Co., Copiague, NY 11726 |
| 29990 | American Technical Ceramics, Div. of Phase Ind. Huntington Station, NY 11746 |
| 32997 | Bourns, Inc, Trimpot Div, Riverside, CA 92507 |
| 34257 | EIP Microwave, Inc., San Jose, CA 95134 |
| 34649 | Intel Corp., Aloha, OR 97005 |
| 35004 | Crouse-Hinds Canada, Ltd., Scarboro, ONT |
| 44655 | Ohmite, Skokie, IL 60076 |
| 51167 | Aries Electronics, Frenchtown, NJ 08825 |
| 51406 | Murata Corp. of America, Marietta, GA 30067 |
| 51640 | Analog Devices, Inc., Wilmington, MA 01887 |
| 51642 | Centre Engineering, State College, PA 16801 |
| 57668 | R-Ohm, Irvine, CA 92213 |
| 56289 | Sprague Electric Co., North Adams, MA 01247 |
| 58317 | Plessey Solid State, Irvine, CA 92714 |

# Appendix A
# List of Manufacturers

| | |
|---|---|
| 59660 | Tusonix Inc., Tucson, AZ 85705 |
| 60395 | Xicor, Inc., Milpitas, CA 95035 |
| 62786 | Hitachi America Ltd, San Jose, CA 95122 |
| 70903 | Belden Corp., Chicago, IL 60644 |
| 71279 | Cambion Div., Midland-Ross Corp., Cambridge, MA 02140 |
| 71590 | Centralab Div., Globe-Union Inc., Milwaukee, WI 53201 |
| 72136 | Electro Motive Corp., Santa Clara, CA 95050 |
| 71895 | Delavan, West Des Moines, IA 50265 |
| 72259 | Nytronics Inc., Pelham Manor, NY 10803 |
| 72982 | Erie Technological Products Inc., Erie, PA 16512 |
| 73445 | Amperex Electronic Corp., Hicksville, NY 11802 |
| 76718 | Nemco Electric Corporation, Seattle, WA 98104 |
| 80031 | Mepco/Electra Inc., Morristown, NJ 07960 |
| 80740 | Beckman Instruments Inc., Fullerton, CA 92634 |
| 81349 | Military Specification |
| 84171 | Arco Electronics, Commack, NY 11725 |
| 86797 | Rogan Bros. Inc., Skokie, IL 60076 |
| 91637 | Dale Electronics Inc., Columbus, NE 68601 |
| 95275 | Vitramon Inc., Bridgeport, CT 06601 |
| 96067 | Microwave Associates, Sunnyvale, CA 94086 |
| 98291 | Sealectro, Mamaroneck, NY 10544 |
| 99800 | Delavan Div., American Precision Industries, East Aurora, NY 14052 |

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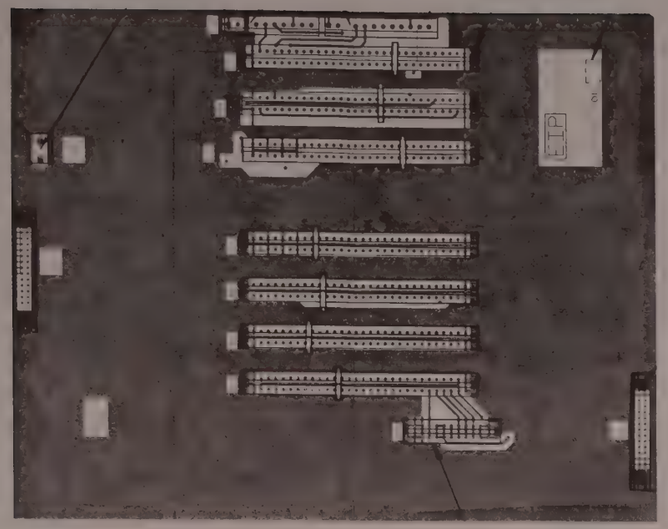


2020221-01

Figure 81-1. Component Locator, Counter Interconnect

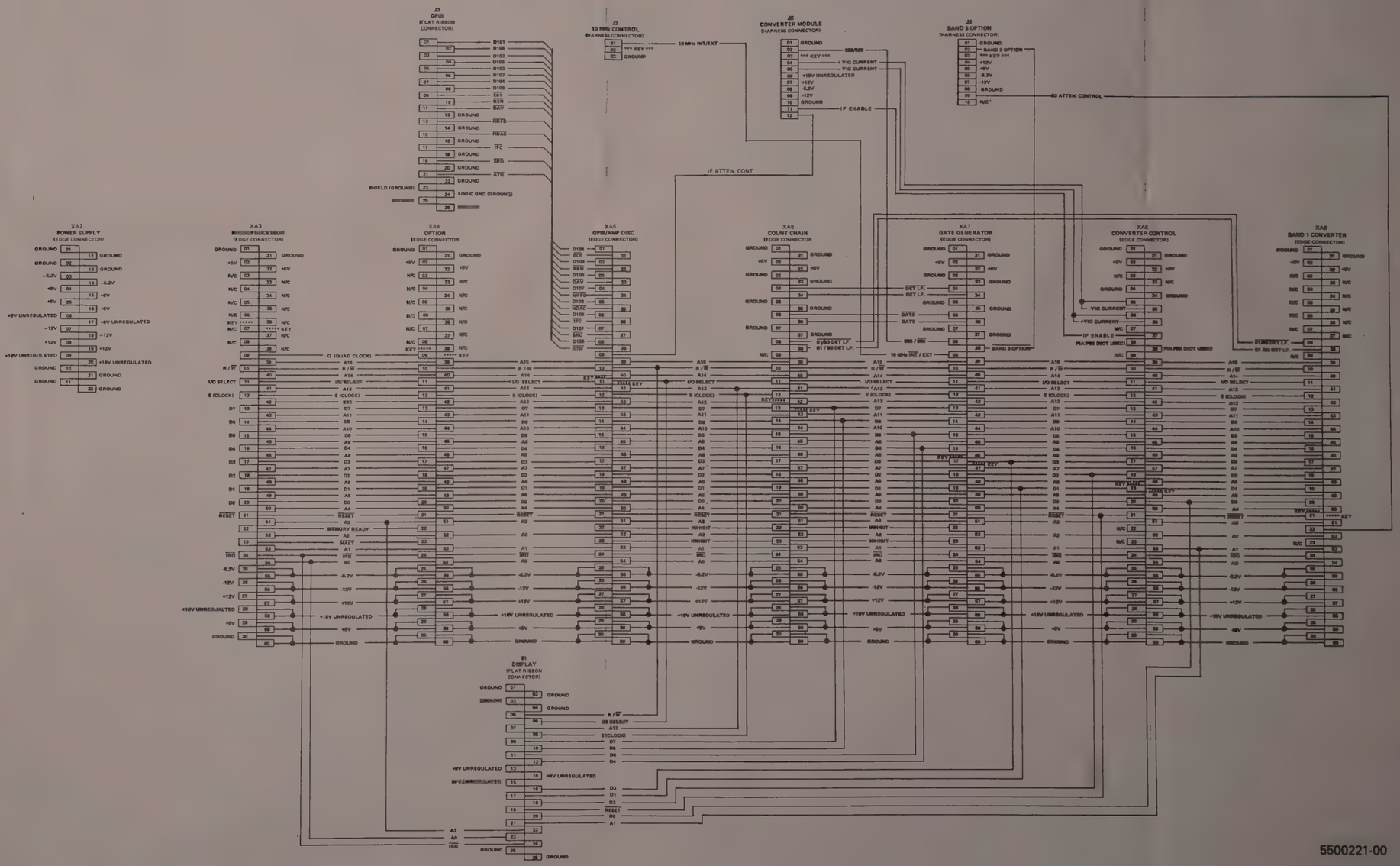



Figure 81-2. Schematic Diagram, Counter Interconnect

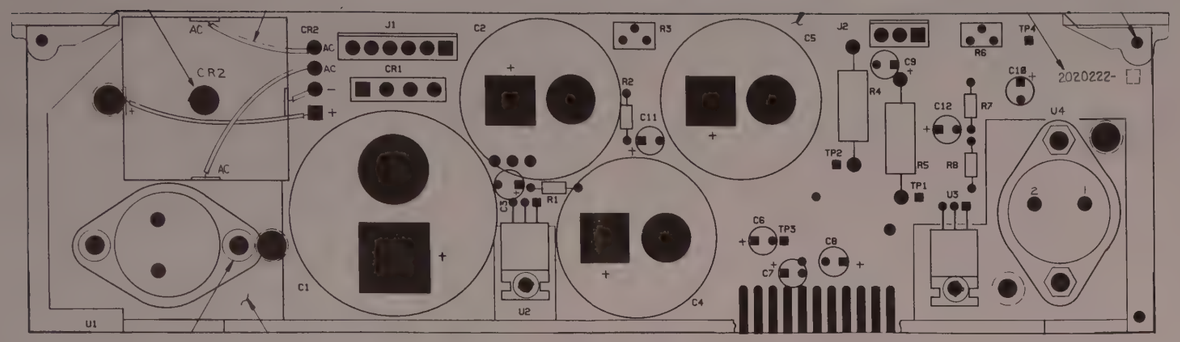



Figure 82-2. Component Locator Power Supply

2020222-01

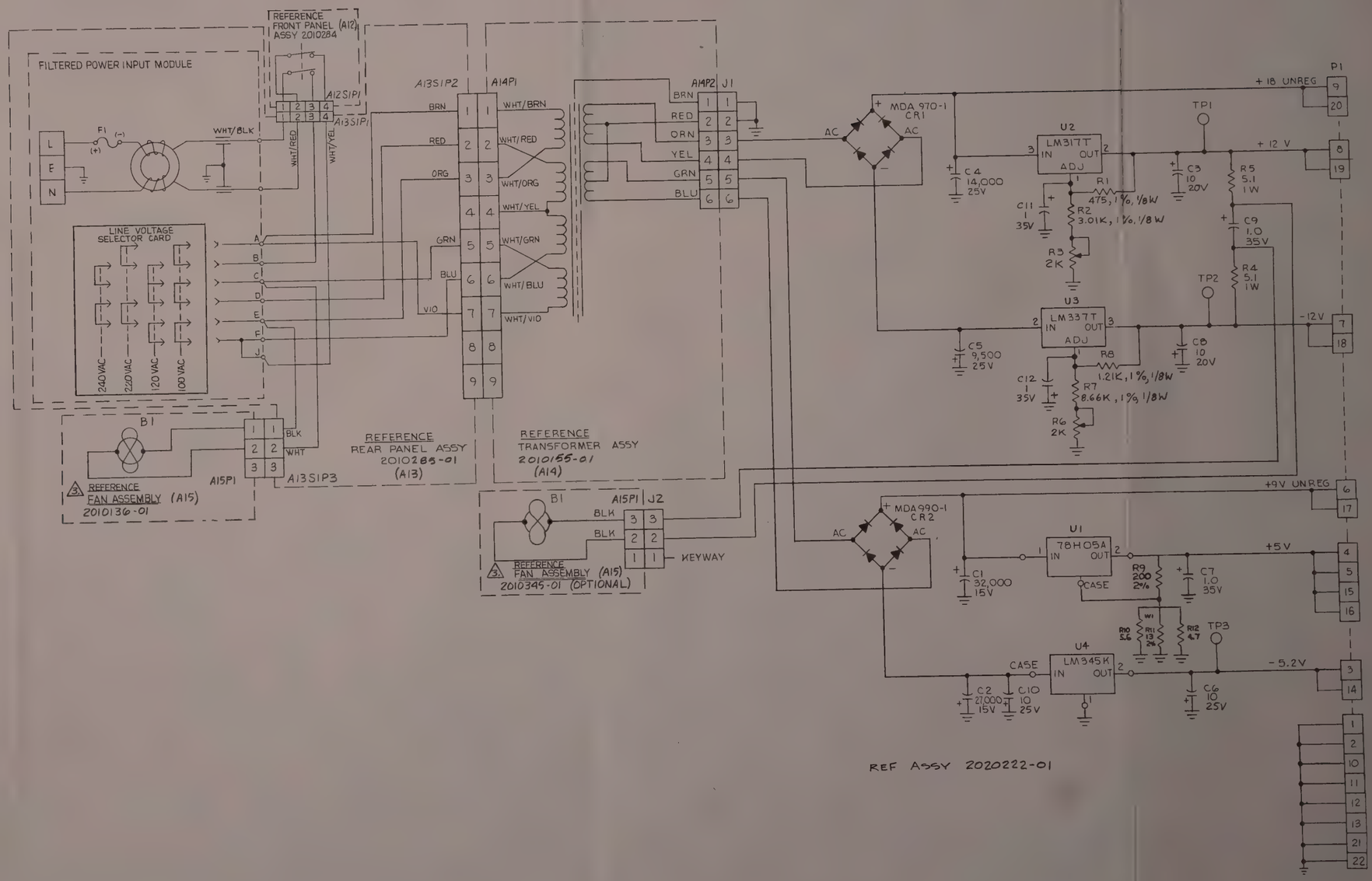



Figure 82-3. Schematic Diagram, Power Supply

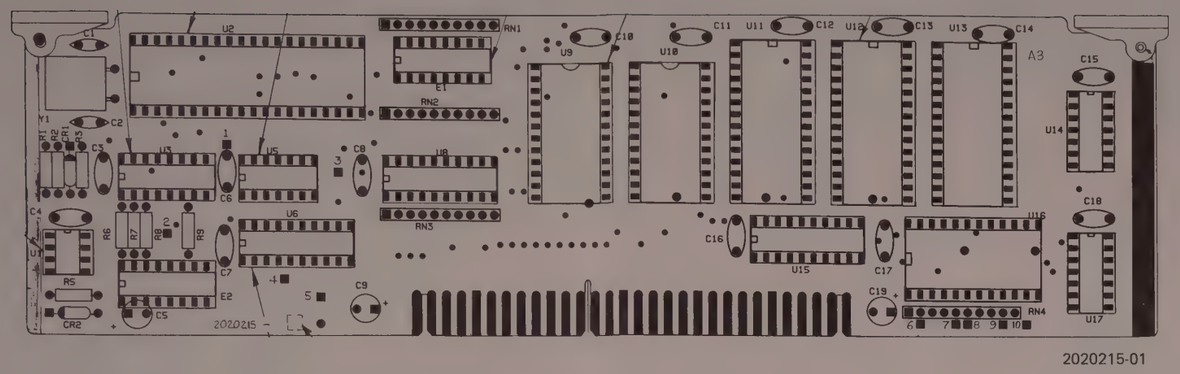



Figure 83-2. Component Locator, Microprocessor

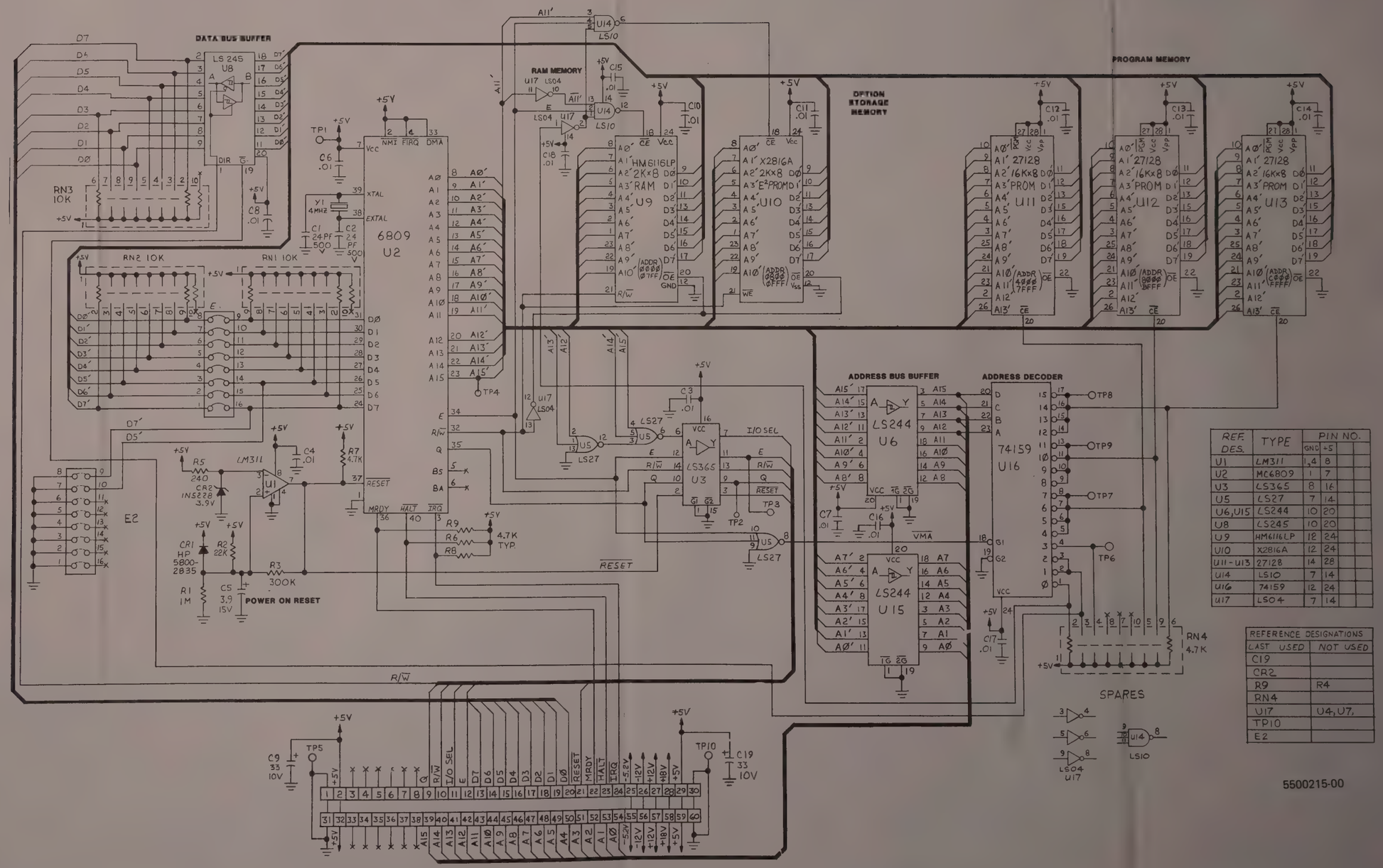



Figure 83-3. Schematic Diagram Microprocessor

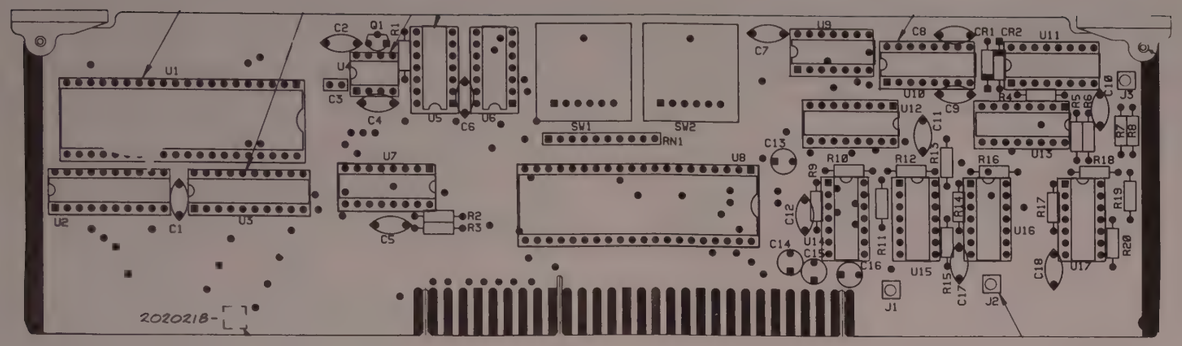
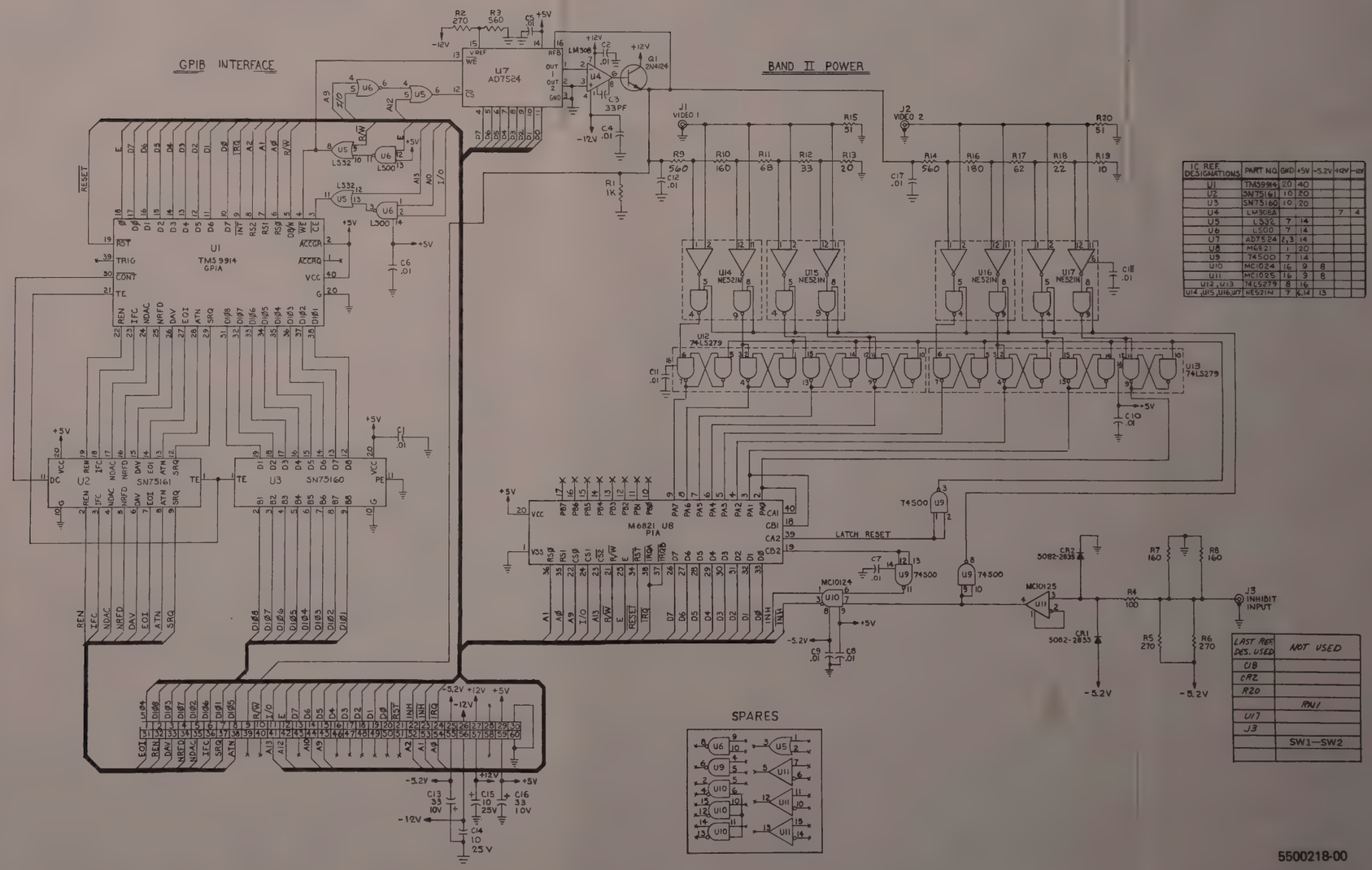



Figure 85-2. Component Locator, GPIB/Band 2 Power Discriminator

2020218-01




| IC REF. DESIGNATIONS | PART NO. | GND | +5V | -5.2V | +12V | -12V |
|---|---|---|---|---|---|---|
| U1 | TMS9914 | 20 | 40 | | | |
| U2 | SN75161 | 10 | 20 | | | |
| U3 | SN75160 | 10 | 20 | | | |
| U4 | LM308A | | | | 7 | 4 |
| U5 | LS32 | 7 | 14 | | | |
| U6 | LS00 | 7 | 14 | | | |
| U7 | AD7524 | 2,3 | 14 | | | |
| U8 | M6821 | 1 | 20 | | | |
| U9 | 74S00 | 7 | 14 | | | |
| U10 | MC10124 | 16 | 9 | 8 | | |
| U11 | MC10125 | 16 | 9 | 8 | | |
| U12, U13 | 74LS279 | 8 | 16 | | | |
| U14, U15, U16, U17 | NE521N | 7 | 8,14 | 13 | | |

| LAST REF DES. USED | NOT USED |
|---|---|
| C18 | |
| CR2 | |
| R20 | |
| | RN1 |
| U17 | |
| J3 | |
| | SW1—SW2 |
| | |

5500218-00

Figure 85-3. Schematic Diagram, GPIB/Band 2 Power Discriminator

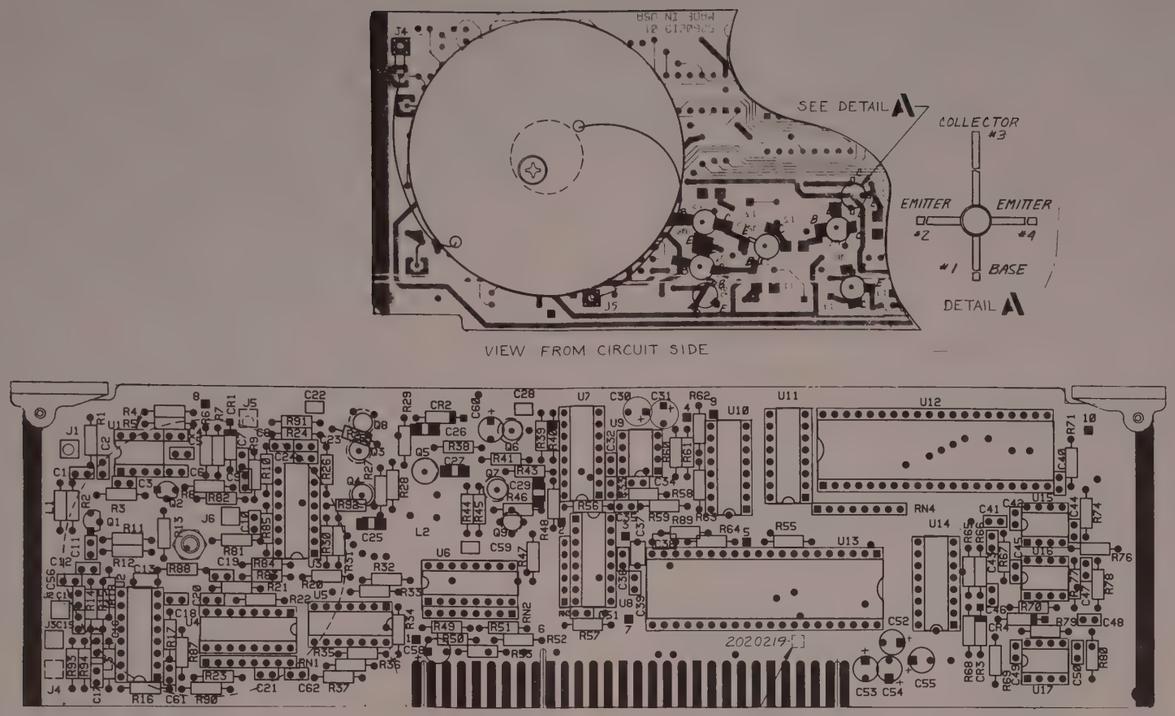
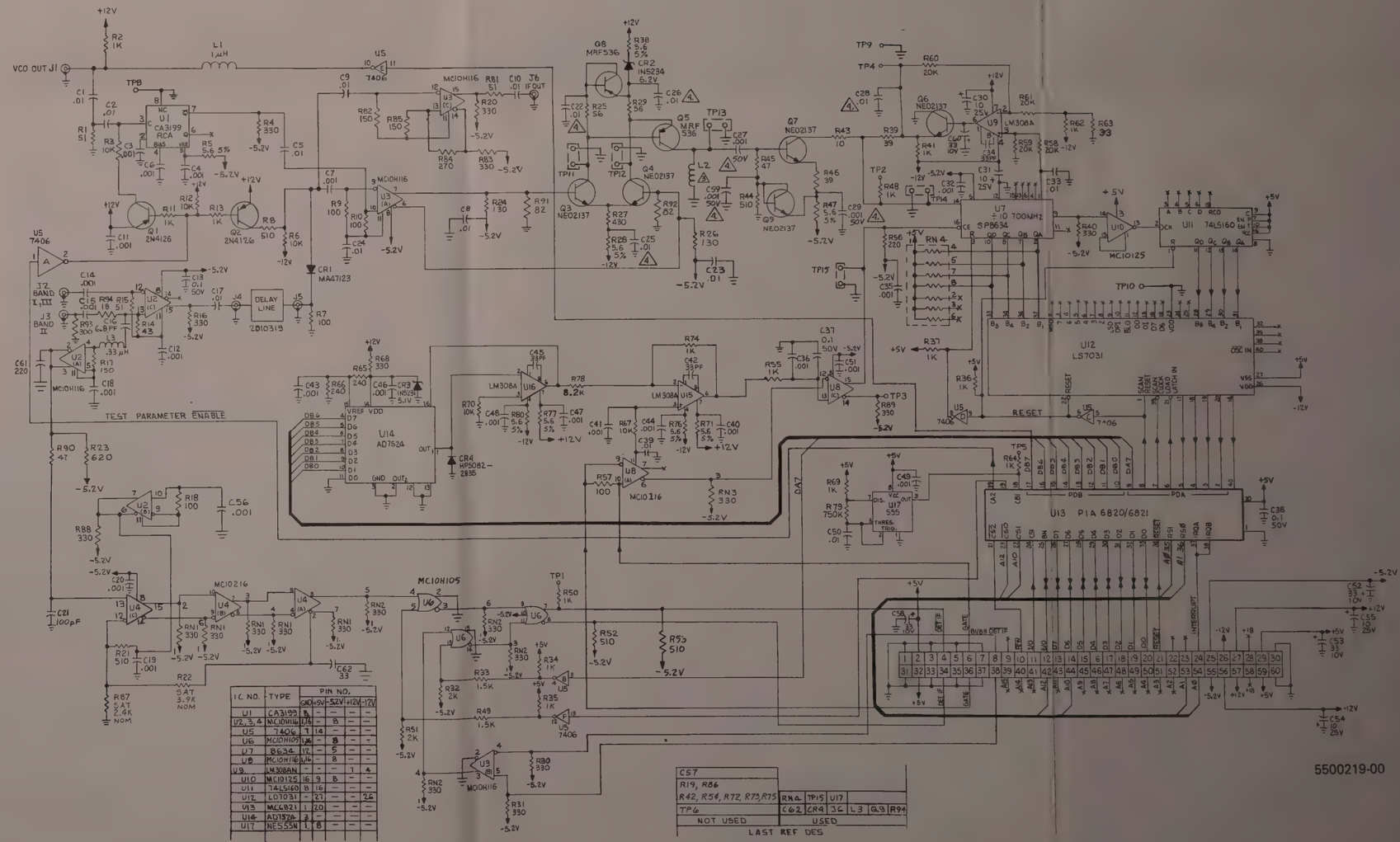



Figure 86-2. Component Locator, Count Chain




| IC NO. | TYPE | PIN NO. GND | +5V | -5.2V | +12V | -12V |
|---|---|---|---|---|---|---|
| U1 | CA3199 | 8 | – | – | – | – |
| U2, 3, 4 | MC10H116 | 8 | – | 8 | – | – |
| U5 | 7406 | 7 | 14 | – | – | – |
| U6 | MC10H105 | 8 | – | 8 | – | – |
| U7 | 8634 | 17 | – | 5 | – | – |
| U8 | MC10H116 | 8 | – | 8 | – | – |
| U9 | LM308AN | – | – | – | 1 | 4 |
| U10 | MC10125 | 16 | 9 | 8 | – | – |
| U11 | 74LS160 | 8 | 16 | – | – | – |
| U12 | LO7031 | – | 21 | – | – | 26 |
| U13 | MCC6821 | 1 | 20 | – | – | – |
| U16 | AD1376 | 2 | – | – | – | – |
| U17 | NE555N | 1 | 8 | – | – | – |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| C57 | | | | | | | |
| R19, R86 | | | | | | | |
| R42, R54, R72, R73, R75 | RN4 | TP15 | U17 | | | | |
| TP6 | C62 | CR4 | J6 | L3 | Q9 | R94 | |
| NOT USED | USED | | | | | | |
| LAST REF DES | | | | | | | |

Figure 86-3. Schematic Diagram, Count Chain

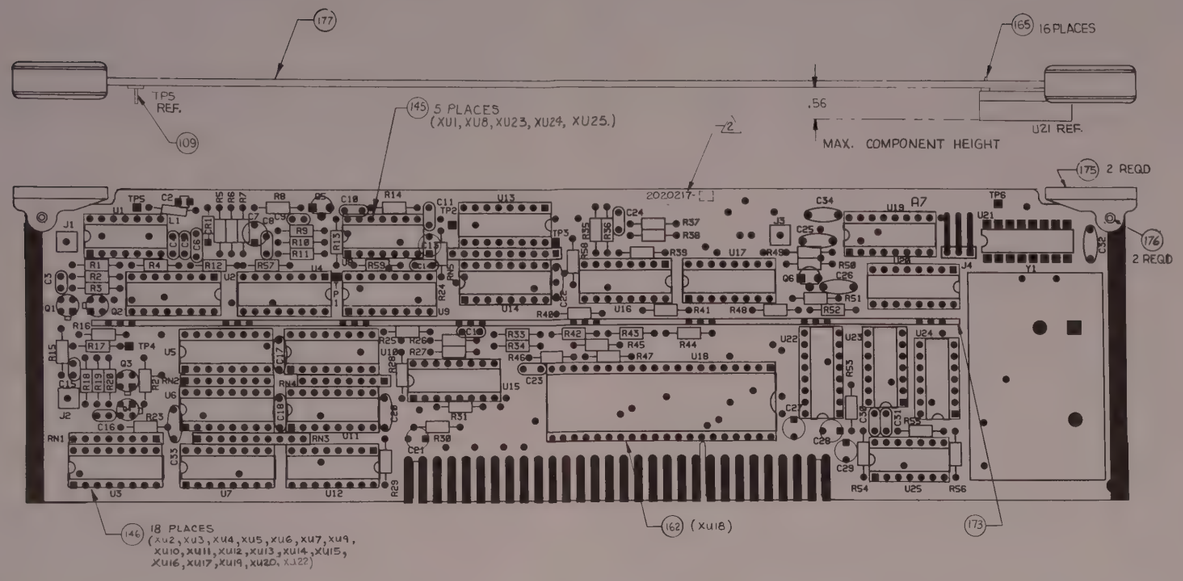
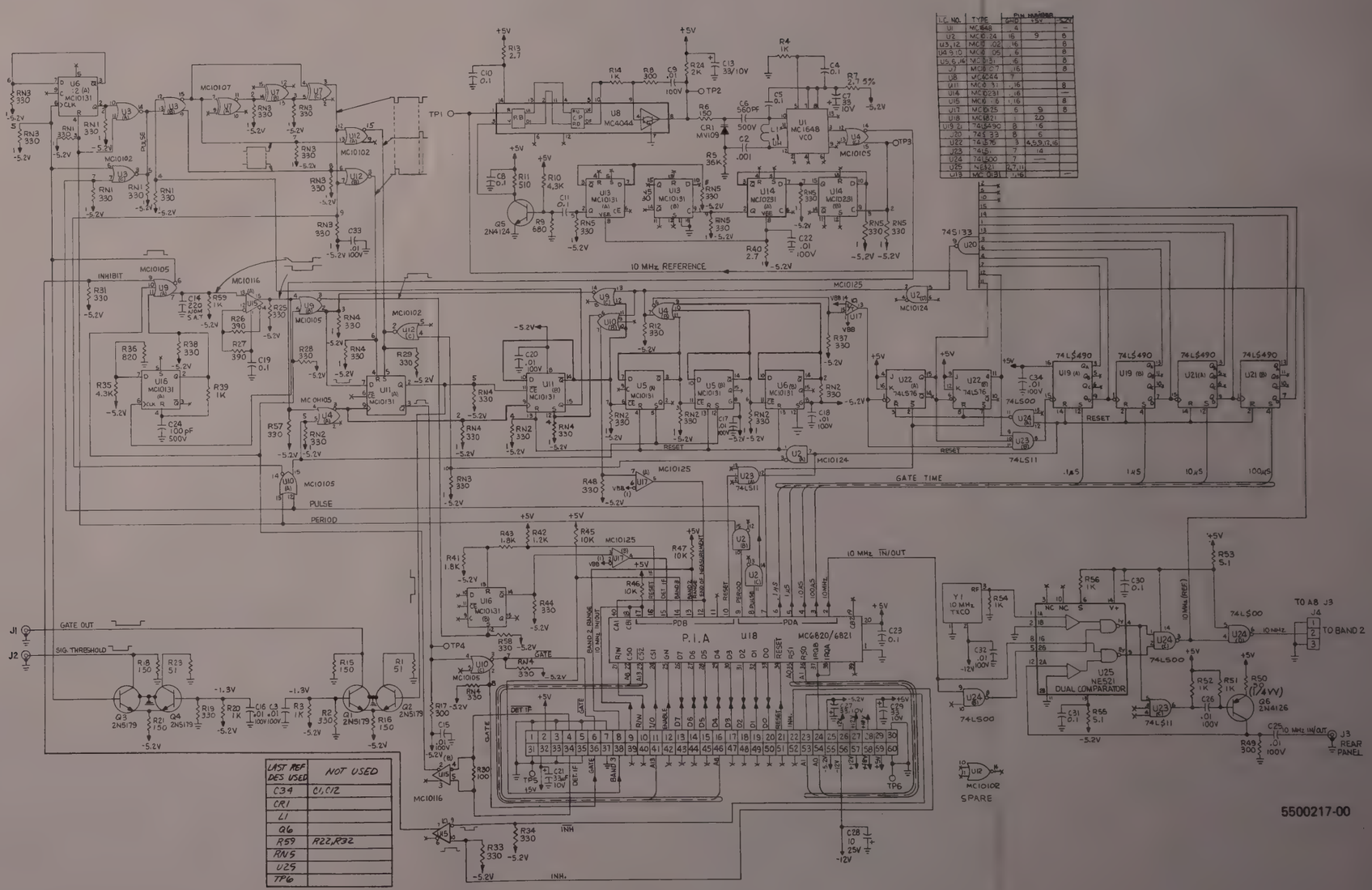



Figure 87-2. Component Locator, Gate Generator

2020217-01




| LAST REF DES USED | NOT USED |
|---|---|
| C34 | C1, C12 |
| CR1 | |
| L1 | |
| Q6 | |
| R59 | R22, R32 |
| RN5 | |
| U25 | |
| TP6 | |

Figure 87-3. Schematic Diagram, Gate Generator

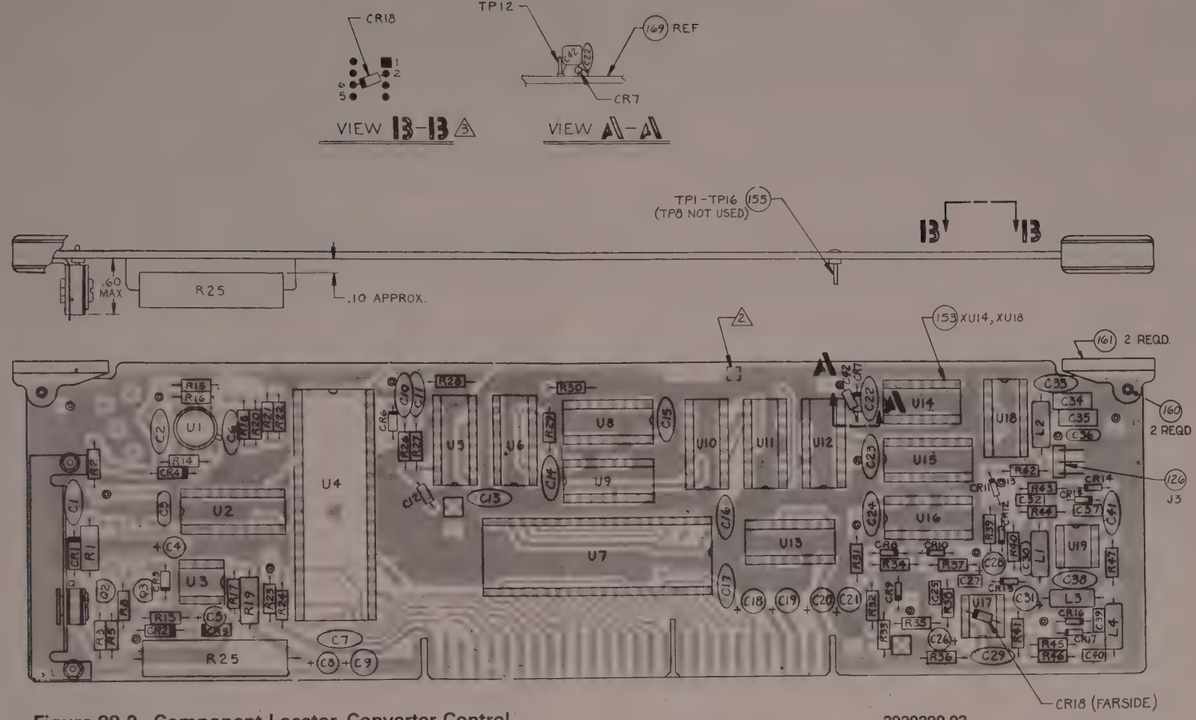
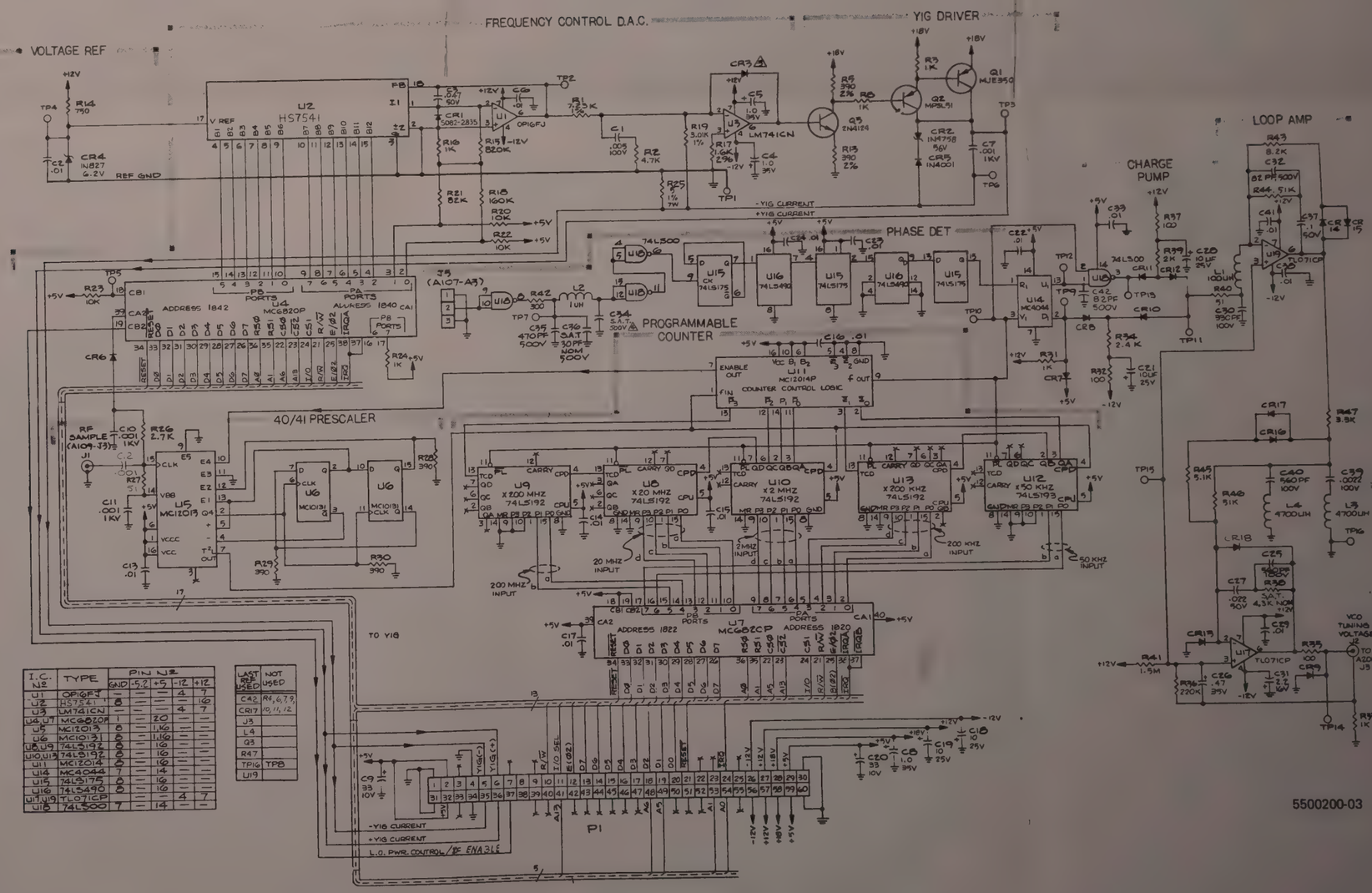



Figure 88-2. Component Locator, Converter Control

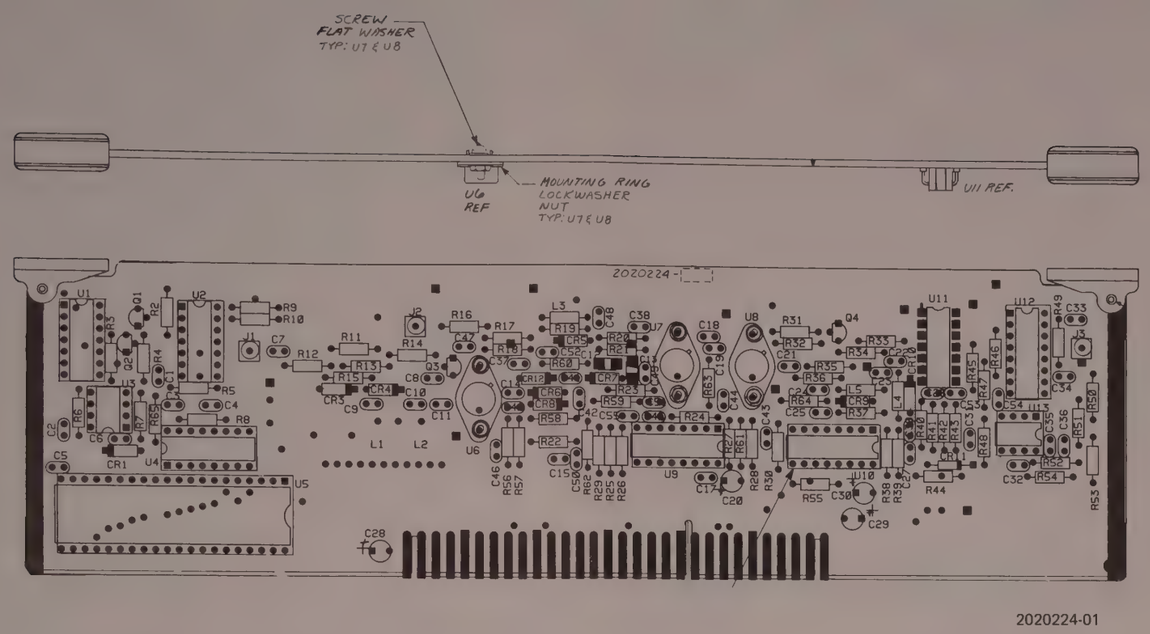
2020200-03




| I.C. No. | TYPE | PIN NO. GND | -5.2 | +5 | -12 | +12 |
|---|---|---|---|---|---|---|
| U1 | OP16FJ | 4 | — | — | 4 | 7 |
| U2 | HS7541 | 8 | — | — | — | 16 |
| U3 | LM741CN | — | — | — | 4 | 7 |
| U4, U7 | MC6820P | 1 | — | 20 | — | — |
| U5 | MC12013 | 8 | — | 16 | — | — |
| U6 | MC10131 | 8 | — | 16 | — | — |
| U8, U9 | 74LS192 | 8 | — | 16 | — | — |
| U10, U13 | 74LS192 | 8 | — | 16 | — | — |
| U11 | MC12014 | 8 | — | 16 | — | — |
| U12 | MC4044 | 7 | — | 14 | — | — |
| U15 | 74LS175 | 8 | — | 16 | — | — |
| U16 | 74LS490 | 8 | — | 16 | — | — |
| U17, U19 | TL071CP | — | — | — | 4 | 7 |
| U18 | 74LS00 | 7 | — | 14 | — | — |

| LAST REF USED | NOT USED |
|---|---|
| C42 | R4, 6, 7, 9 |
| CR17 | 10, 11, 12 |
| J3 | |
| L4 | |
| Q3 | |
| R47 | |
| TP16 | TP8 |
| U19 | |

Figure 88-3. Schematic Diagram, Converter Control




2020224-01

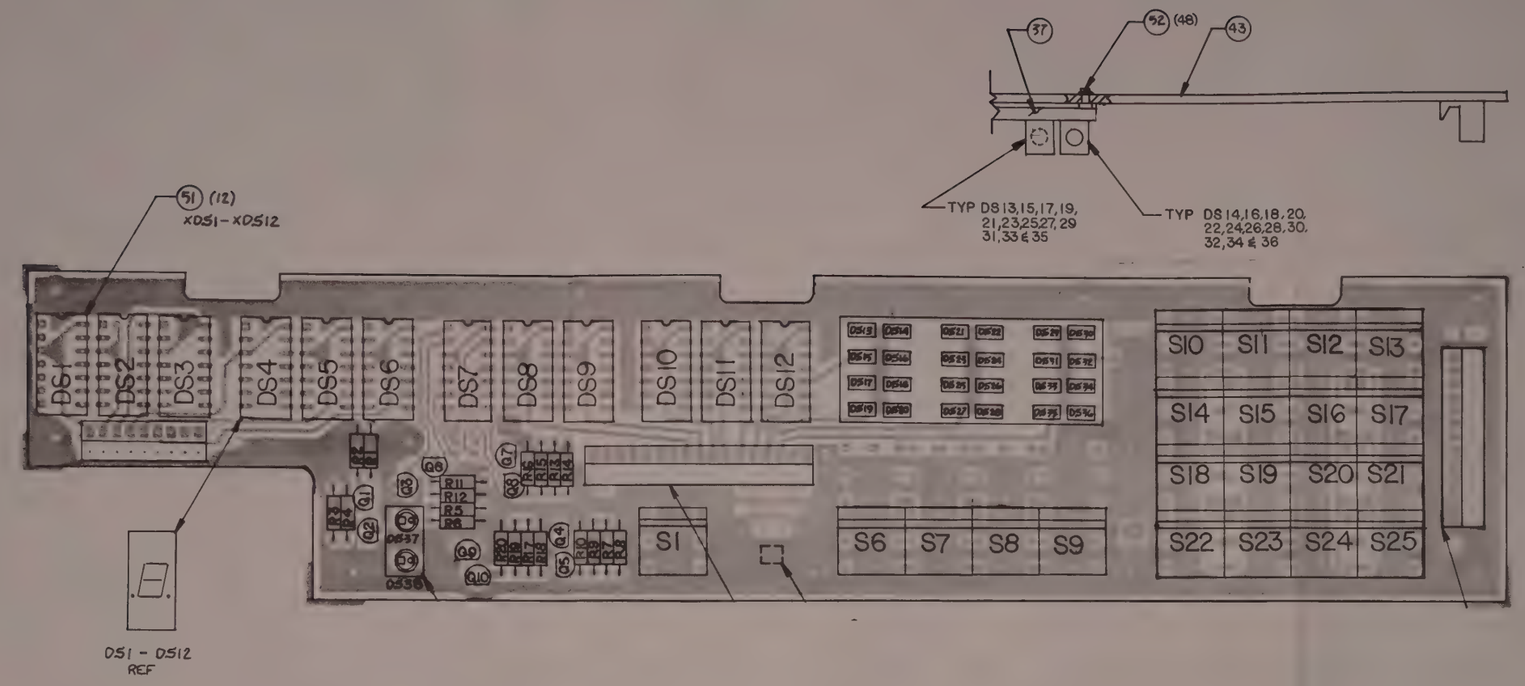
Figure 89-2. Component Locator, Band 1 Converter (Option)

| IC. No. | TYPE | PIN NO. | | | | |
|---|---|---|---|---|---|---|
| | | +5V | -5.2V | +12V | -12V | GND |
| U1 | 7406 | 14 | — | — | — | 7 |
| U2 | MC14066B | — | — | 14 | — | 7 |
| U3, U13 | LM308 | — | — | — | — | — |
| U4 | AD7524LN | 14 | — | — | — | 2,3,12,13 |
| U5 | MC6820P | 20 | — | — | — | 1 |
| U6, U7, U8 | GPD-1003/1063 | — | — | — | — | 3 |
| U9, U10, U12 | MC10H116 | — | 8 | — | — | 1,16 |
| U11 | SP8617B | — | 9 | — | — | 14 |
| | | | | | | |

| LAST REF DES USED | NOT USED |
|---|---|
| C54 | C16 |
| CR12 | CR2 |
| R69 | R1 |
| U13 | |
| TP13 | |
| J3 | |
| L5 | |
| Q4 | |
| | |

5500224-00

Figure 89-3. Schematic Diagram, Band 1 Converter (Option)




2020140-02

**Figure 812A1-1. Component Locator, Front Panel Display/Keyboard**

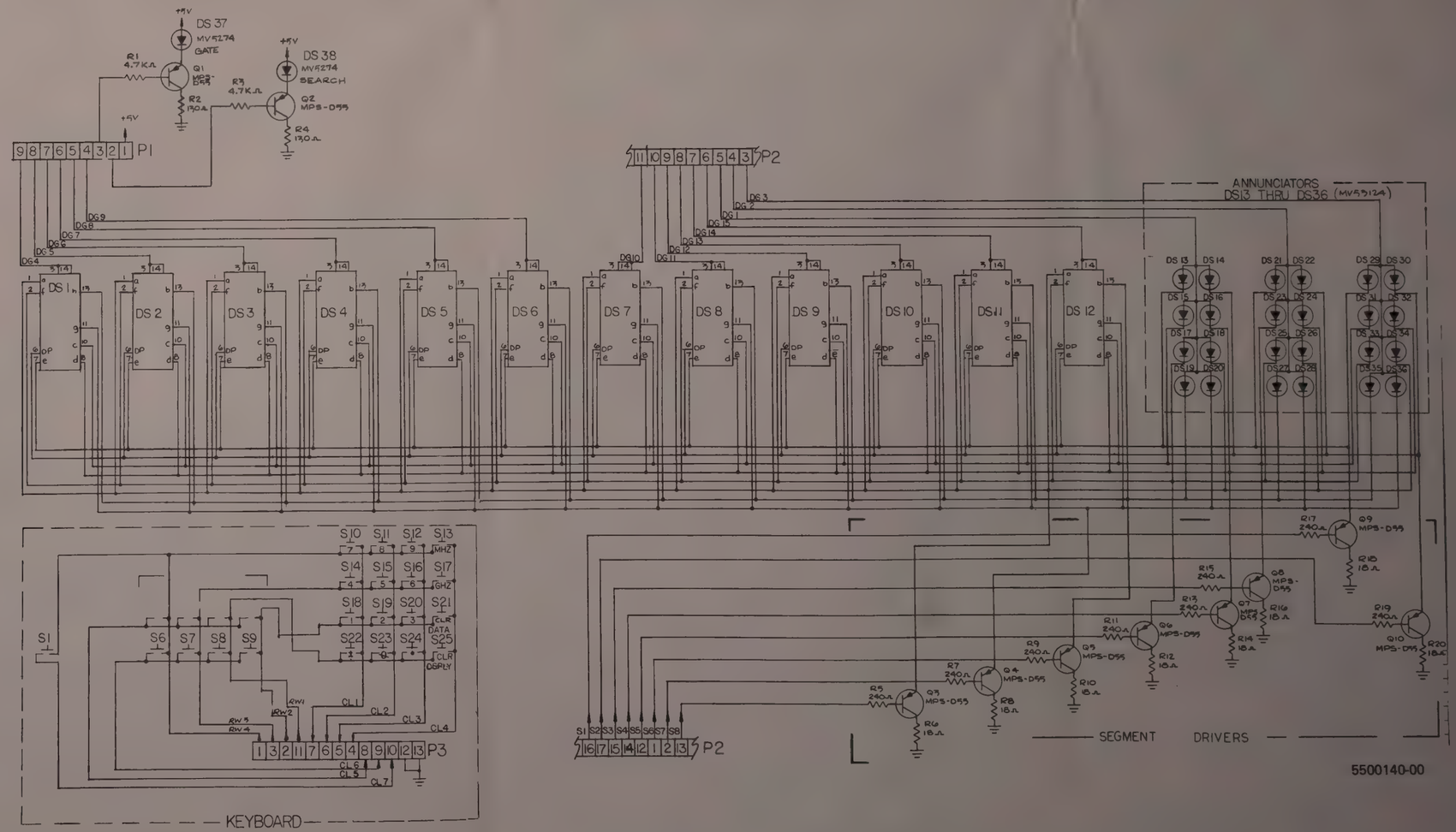



**Figure 812A1-2. Schematic Diagram, Front Panel Display/Keyboard**

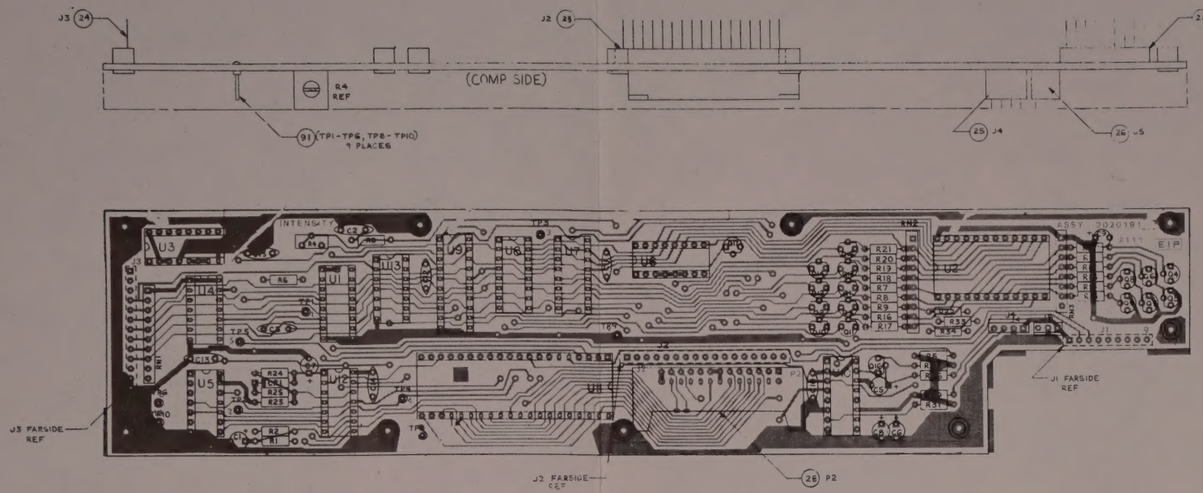
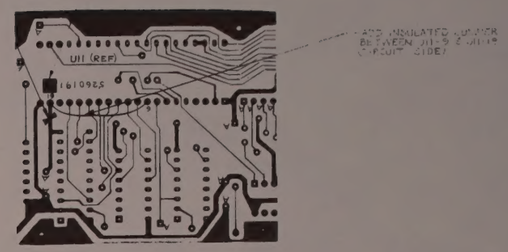



Figure 812A2-3. Component Locator, Front Panel Logic

2020191-02



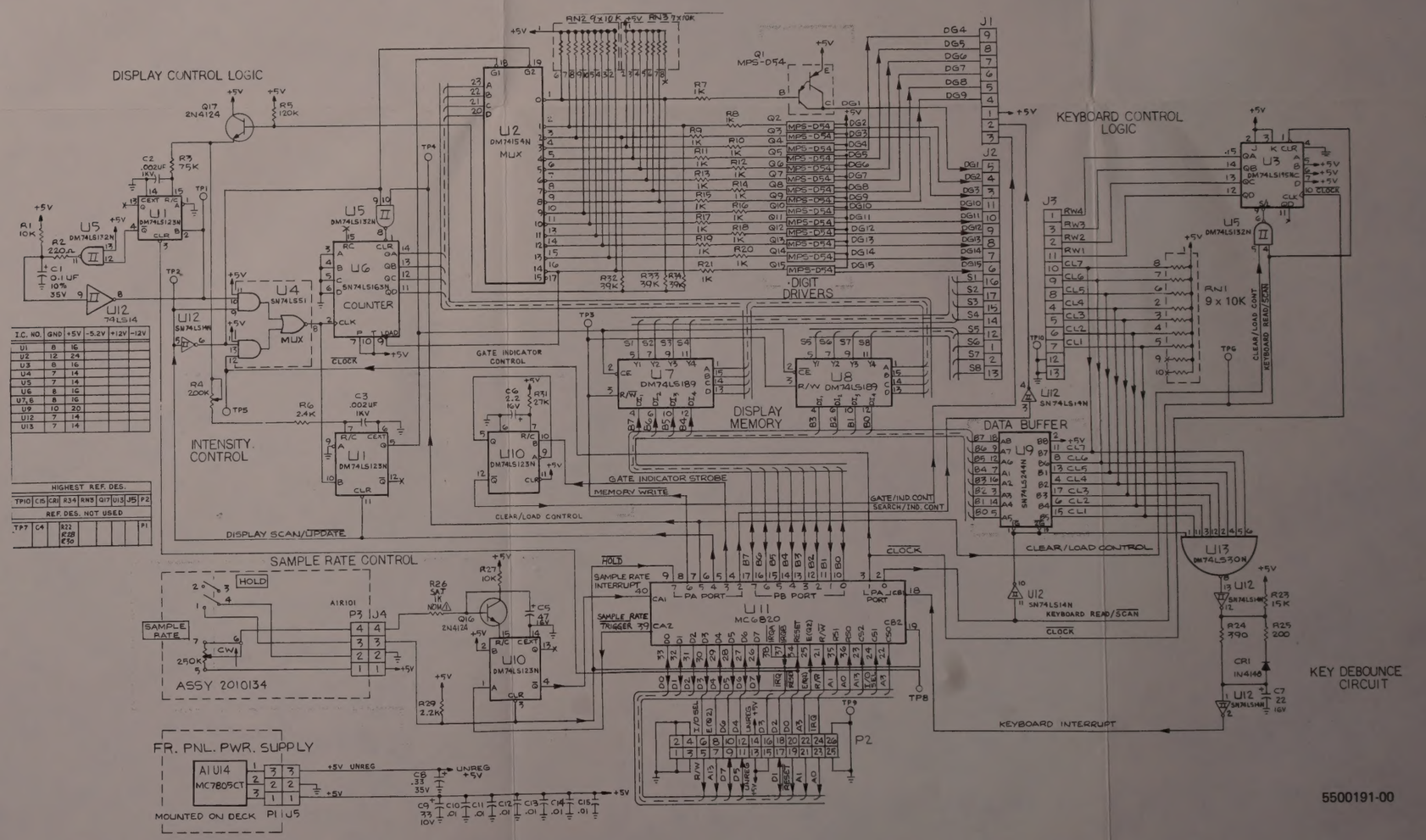




Figure 812A2-4. Schematic Diagram, Front Panel Logic

5500191-00